



B75H2-AD

Rev : 1.0.

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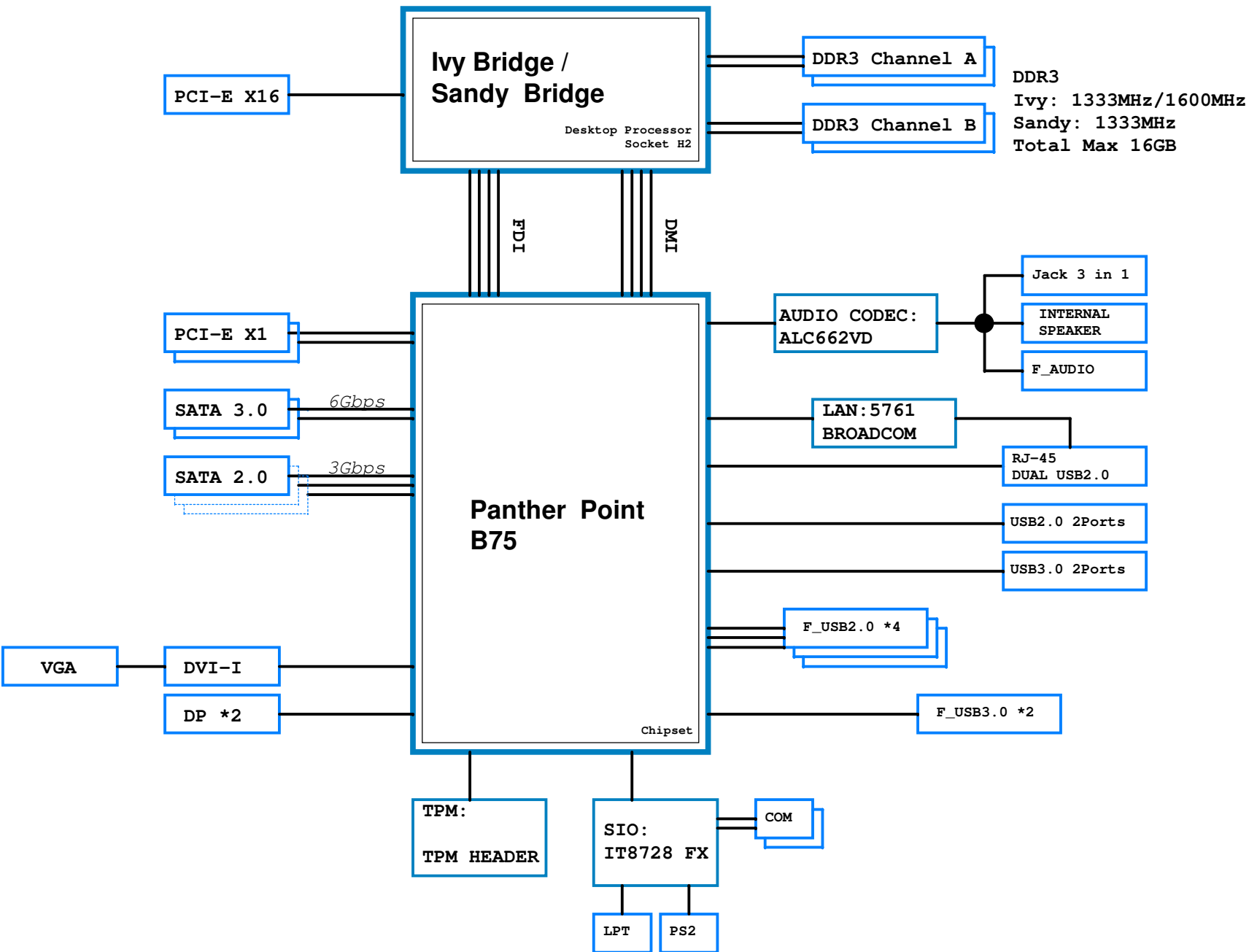
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REVISION HISTORY:

Rev	Date	Notes
V.A	2011/10/03	Initial version
V.B	2011/12/13	
V1.0	2012/01/17	
V1.0.	2012/04/10	

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GPIO Table

PCH

Name	Type	Voltage	Default	Function
GPIO1	I/O	+VCC3	Input	OBR
GPIO6	I/O	+VCC3	Input	Thermal Shut Down
GPIO13	I/O	+3VSB	Input	LPC_PME_L
GPIO15	I/O	+3VSB	Input	TLS_EN
GPIO23	I/O	+VCC3	Input	HDPANEL_DETECT
GPIO27	I/O	SB_3VSB	Input	LANWAKEB for Bcm
GPIO28	I/O	+3VSB	Input	ON_DIE_PLL_EN
GPIO45	I/O	+3VSB	Input	SPI_WPSW
GPIO57	I/O	+3VSB	Input	SPI_WP0_L
GPIO59	I/O	+3VSB	Input	LAN_LED_D
GPIO61	I/O	+3VSB	Input	LPCPD_L
GPIO72	I/O	+3VSB	Input	GPIO72_S4S5

IT8728F D/EX

Name	Type	Voltage	Int. Res.	Function
GP14	I/O	+VCC3	OD	Thermal Shut Down
GP15	I/O	+VCC3	OD	MB_ID1
GP16	I/O	+VCC3	OD	PC BEEP
GP22	I/O	+3VSB	OD	LED1
GP23	I/O	+3VSB	OD	LED0
GP35	I/O	+VCC3	OD	MB_ID2
GP36	I/O	+VCC3	OD	GPO36 FOR ACER reserve
GP64	I/O	+VCC3	OD	GPO64 FOR ACER reserve

Straping Table

PCH Straping (Page.14)

TLS Confidentiality:

TLS_EN (internal PD)	
H	Enable TLS
L	Disable TLS

No Reboot:

PCH_SPKR (internal PD)	
H	Enable No Reboot
L	Disable

On-Die PLL VR:

ON_DIE_PLL_EN (internal PU)	
H	Enable
L	Disable

On-Die PLL VR Source:

HDA_SYNC_R (internal PD)	
H	1.5V
L	1.8V

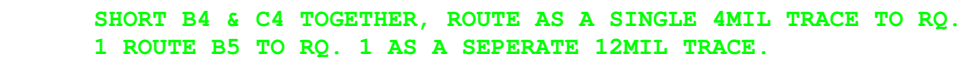
Integrated 1.05V SUS VRM:

INTVRMEN	
H	Enable
L	Disable

SIO IT8728F D/EX Straping (Page.28)

Power-On Strapping

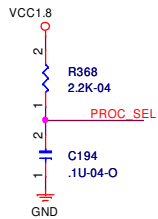
	Symbol	Value	Description
JP1 Pin-48	DSW_EUP_SEL	1	EUP
		0	DSW
JP2 Pin-122	WDT_EN	1	Disable WDT to reset PWROK
		0	Enable WDT to reset PWROK
JP3 Pin-124	FAN_CTL_SEL	1	EC Index 63h/6Bh/73h is 80h
		0	EC Index 63h/6Bh/73h is 00h
JP4 Pin-126	K8PWR_EN	1	Disable K8 Power Sequence
		0	Enable K8 Power Sequence
JP5 Pin-29	UOVMODE_SEL	1	Notice Mode (Default)
	OV/UV	0	Force Mode



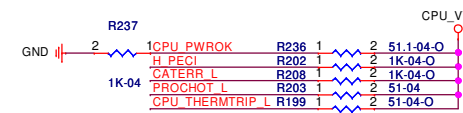
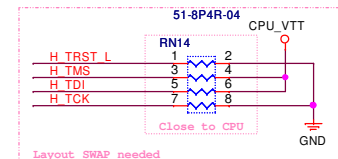
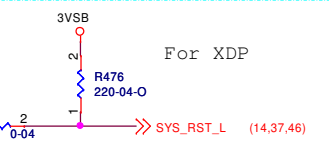
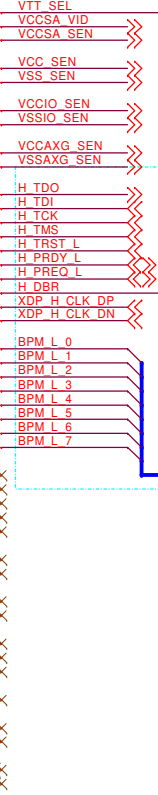
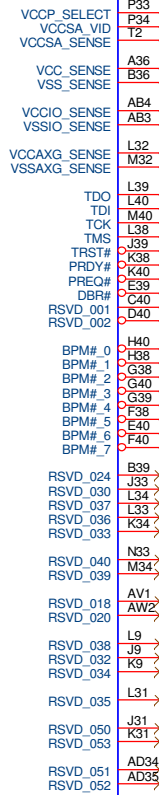
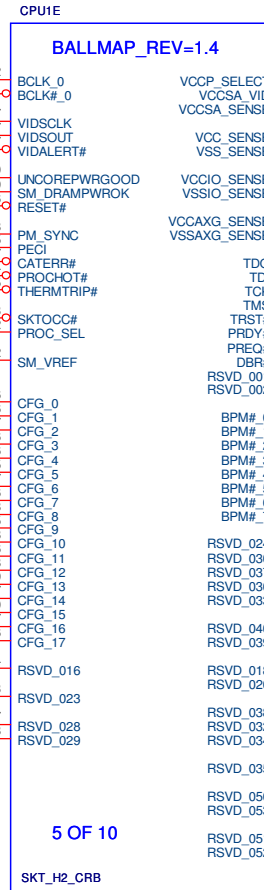
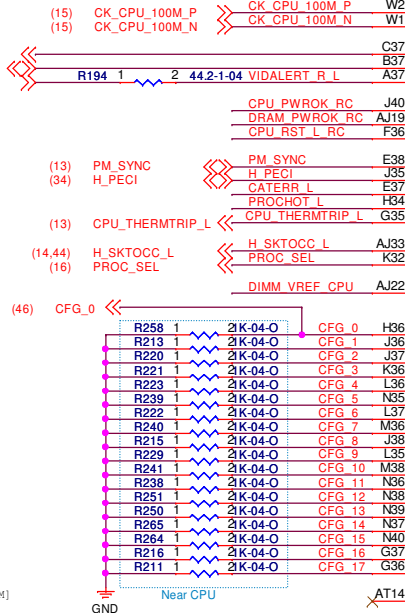
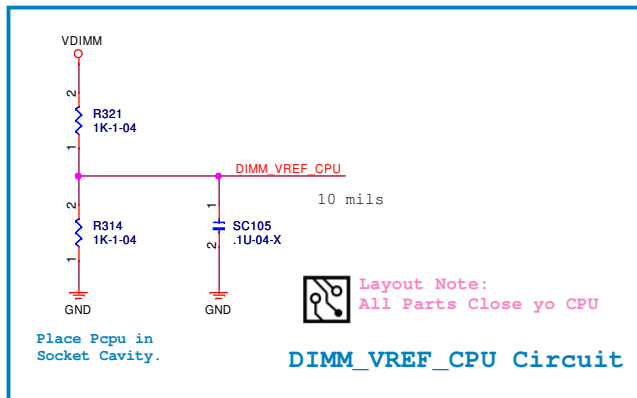
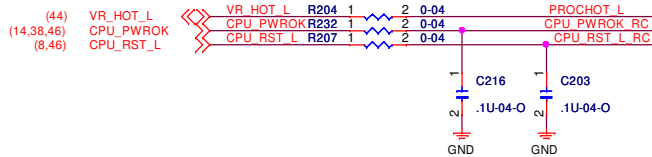
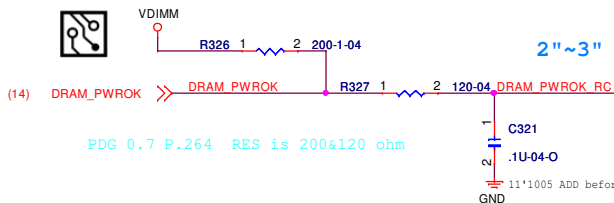
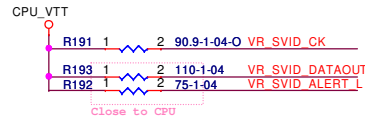
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DMI/FDI TERMINATION VOLTAGE
 DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
 DC COUPLED: TX/RX TO VSS IF SAMPLED LOW
 AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFGSEL[0]
6	*	*	PEOFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

PCIE CONFIG	SEL0	SEL1
1 X 16	1	1
2 X 8	0	1

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CPU - MISC

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CFG_0..17 HAVE INTERNAL PULL-UPS

(9)	M_DATA_A[0..63]	←	M_DATA A[0..63]
(9)	M_DQS_A_P[0..7]	←	M DQS A P[0..7]
(9)	M_DQS_A_N[0..7]	←	M DQS A N[0..7]
(9)	M_MA_A[0..15]	←	M MA A[0..15]
(9)	M_MA_A[0..15]	←	M BS A[0..2]
(9)	M_BS_A[0..2]	←	M CS A L[0..3]
(9)	M_CS_A_L[0..3]	←	M_CKE A[0..3]
(9)	M_CKE_A[0..3]	←	M_ODT A[0..3]
(9)	M_ODT_A[0..3]	←	M_CLK A P[0..3]
(9)	M_CLK_A_P[0..3]	←	M_CLK A N[0..3]
(9)	M_CLK_A_N[0..3]	←	M WE A L
(9)	M_WE_A_L	←	M CAS A L
(9)	M_CAS_A_L	←	M RAS A L
(9)	M_RAS_A_L	←	

DDR3 CH.A

(9,10) DDR3_DRAMRST_L ← DDR3_DRAMRST_L

(10)	M_DATA_B[0..63]	←	M_DATA B[0..63]
(10)	M_DQS_B_P[0..7]	←	M DQS B P[0..7]
(10)	M_DQS_B_N[0..7]	←	M DQS B N[0..7]
(10)	M_MA_B[0..15]	←	M MA B[0..15]
(10)	M_MA_B[0..15]	←	M BS B[0..2]
(10)	M_BS_B[0..2]	←	M CS B L[0..3]
(10)	M_CS_B_L[0..3]	←	M_CKE B[0..3]
(10)	M_CKE_B[0..3]	←	M_ODT B[0..3]
(10)	M_ODT_B[0..3]	←	M_CLK B P[0..3]
(10)	M_CLK_B_P[0..3]	←	M_CLK B N[0..3]
(10)	M_CLK_B_N[0..3]	←	M WE B L
(10)	M_WE_B_L	←	M CAS B L
(10)	M_CAS_B_L	←	M RAS B L
(10)	M_RAS_B_L	←	

DDR3 CH.B

BALLMAP_REV=1.4			
M_DATA A0	AJ3	SA_DQ_0	AV27
M_DATA A1	AJ4	SA_DQ_1	AV24
M_DATA A2	AL3	SA_DQ_2	AW24
M_DATA A3	AL4	SA_DQ_3	AW23
M_DATA A4	AJ2	SA_DQ_4	AV23
M_DATA A5	AJ1	SA_DQ_5	AT24
M_DATA A6	AL1	SA_DQ_6	AV23
M_DATA A7	AL1	SA_DQ_7	AV22
M_DATA A8	AN1	SA_DQ_8	AT22
M_DATA A9	AN4	SA_DQ_9	AV28
M_DATA A10	AR3	SA_DQ_10	AT21
M_DATA A11	AR4	SA_DQ_11	AW32
M_DATA A12	AN2	SA_DQ_12	AU22
M_DATA A13	AN3	SA_DQ_13	AV22
M_DATA A14	AR2	SA_DQ_14	AT22
M_DATA A15	AR1	SA_DQ_15	AV28
M_DATA A16	AV2	SA_DQ_16	AT21
M_DATA A17	AV3	SA_DQ_17	AW32
M_DATA A18	AV5	SA_DQ_18	AT20
M_DATA A19	AW5	SA_DQ_19	SA_WE#
M_DATA A20	AU2	SA_DQ_20	SA_CAS#
M_DATA A21	AU3	SA_DQ_21	SA_RAS#
M_DATA A22	AU5	SA_DQ_22	
M_DATA A23	AV5	SA_DQ_23	
M_DATA A24	AY7	SA_DQ_24	
M_DATA A25	AU7	SA_DQ_25	
M_DATA A26	AV9	SA_DQ_26	
M_DATA A27	AU9	SA_DQ_27	
M_DATA A28	AV7	SA_DQ_28	
M_DATA A29	AW7	SA_DQ_29	
M_DATA A30	AW9	SA_DQ_30	
M_DATA A31	AY9	SA_DQ_31	
M_DATA A32	AU35	SA_DQ_32	
M_DATA A33	AW37	SA_DQ_33	
M_DATA A34	AU39	SA_DQ_34	
M_DATA A35	AU36	SA_DQ_35	
M_DATA A36	AW35	SA_DQ_36	
M_DATA A37	AY36	SA_DQ_37	
M_DATA A38	AU38	SA_DQ_38	
M_DATA A39	AU37	SA_DQ_39	
M_DATA A40	AR40	SA_DQ_40	
M_DATA A41	AR37	SA_DQ_41	
M_DATA A42	AN38	SA_DQ_42	
M_DATA A43	AN37	SA_DQ_43	
M_DATA A44	AR39	SA_DQ_44	
M_DATA A45	AR38	SA_DQ_45	
M_DATA A46	AR39	SA_DQ_46	
M_DATA A47	AN40	SA_DQ_47	
M_DATA A48	AL40	SA_DQ_48	
M_DATA A49	AL37	SA_DQ_49	
M_DATA A50	AJ38	SA_DQ_50	
M_DATA A51	AJ37	SA_DQ_51	
M_DATA A52	AL39	SA_DQ_52	
M_DATA A53	AL38	SA_DQ_53	
M_DATA A54	AJ39	SA_DQ_54	
M_DATA A55	AJ40	SA_DQ_55	
M_DATA A56	AG40	SA_DQ_56	
M_DATA A57	AG37	SA_DQ_57	
M_DATA A58	AE38	SA_DQ_58	
M_DATA A59	AE37	SA_DQ_59	
M_DATA A60	AG39	SA_DQ_60	
M_DATA A61	AG38	SA_DQ_61	
M_DATA A62	AE39	SA_DQ_62	
M_DATA A63	AE40	SA_DQ_63	
M_DQS A P0	AK3	SA_DQS_0	AV13
M_DQS A P1	AP3	SA_DQS_1	AV12
M_DQS A P2	AW4	SA_DQS_2	
M_DQS A P3	AV8	SA_DQS_3	
M_DQS A P4	AV37	SA_DQS_4	
M_DQS A P5	AP38	SA_DQS_5	
M_DQS A P6	AK38	SA_DQS_6	
M_DQS A P7	AF38	SA_DQS_7	
M_DQS A N0	AK2	SA_DQS#_0	
M_DQS A N1	AP2	SA_DQS#_1	
M_DQS A N2	AV4	SA_DQS#_2	
M_DQS A N3	AW5	SA_DQS#_3	
M_DQS A N4	AV26	SA_DQS#_4	
M_DQS A N5	AP39	SA_DQS#_5	
M_DQS A N6	AK39	SA_DQS#_6	
M_DQS A N7	AF39	SA_DQS#_7	

SM_DRAMRST#

SA_DQS_8

SA_ECC_CB_0
SA_ECC_CB_1
SA_ECC_CB_2
SA_ECC_CB_3
SA_ECC_CB_4
SA_ECC_CB_5
SA_ECC_CB_6
SA_ECC_CB_7

DDR_0

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SKT_H2_CRB

DDR3 CH.A

SA_MA_0	AV24	M MA A1
SA_MA_1	AJ9	M MA A2
SA_MA_2	AW23	M MA A3
SA_MA_3	AV23	M MA A4
SA_MA_4	AT24	M MA A5
SA_MA_5	AV23	M MA A6
SA_MA_6	AV22	M MA A7
SA_MA_7	AT22	M MA A8
SA_MA_8	AV28	M MA A9
SA_MA_9	AT21	M MA A10
SA_MA_10	AW32	M MA A11
SA_MA_11	AU22	M MA A12
SA_MA_12	AV22	M MA A13
SA_MA_13	AT22	M MA A14
SA_MA_14	AV28	M MA A15
SA_MA_15		
SA_WE#	AW29	M WE A L
SA_CAS#	AV30	M CAS A L
SA_RAS#	AU28	M RAS A L
SA_BS_0	AV29	M BS A0
SA_BS_1	AV20	M BS A2
SA_BS_2		
SA_CS#_0	AJ29	M CS A L0
SA_CS#_1	AV32	M CS A L1
SA_CS#_2	AW30	M CS A L2
SA_CS#_3	AU33	M CS A L3
SA_CKE_0	AV19	M CKE A0
SA_CKE_1	AU18	M CKE A1
SA_CKE_2	AV18	M CKE A3
SA_CKE_3		
SA_ODT_0	AV31	M ODT A0
SA_ODT_1	AU32	M ODT A1
SA_ODT_2	AU30	M ODT A2
SA_ODT_3	AW33	M ODT A3
SA_CK_0	AY25	M CLK A P0
SA_CK#_0	AW25	M CLK A N0
SA_CK_1	AJ24	M CLK A P1
SA_CK#_1	AU25	M CLK A N1
SA_CK_2	AW27	M CLK A P2
SA_CK#_2	AY27	M CLK A N2
SA_CK_3	AV26	M CLK A P3
SA_CK#_3	AW26	M CLK A N3
AW18	DDR3_DRAMRST_R L	
AV13		
AV12		
AU12		
AU14		
AW13		
AY13		
AU11		
AY12		
AW12		

Desktop dosen't support ECC



For RC Filter

Pay Attention to This Part!

M_DATA B0	AG7	SB_DO_0
M_DATA B1	AG8	SB_DO_1
M_DATA B2	AJ8	SB_DO_2
M_DATA B3	AG5	SB_DO_3
M_DATA B4	AG6	SB_DO_4
M_DATA B5	AL6	SB_DO_5
M_DATA B6	AJ7	SB_DO_6
M_DATA B7	AL7	SB_DO_7
M_DATA B8	AM7	SB_DO_8
M_DATA B9	AM10	SB_DO_9
M_DATA B10	AL10	SB_DO_10
M_DATA B11	AL10	SB_DO_11
M_DATA B12	AL6	SB_DO_12
M_DATA B13	AL9	SB_DO_13
M_DATA B14	AM9	SB_DO_14
M_DATA B15	AP7	SB_DO_15
M_DATA B16	AP7	SB_DO_16
M_DATA B17	AP10	SB_DO_17
M_DATA B18	AR10	SB_DO_18
M_DATA B19	AP6	SB_DO_19
M_DATA B20	AR6	SB_DO_20
M_DATA B21	AP9	SB_DO_21
M_DATA B22	AM12	SB_DO_22
M_DATA B23	AM13	SB_DO_23
M_DATA B24	AR13	SB_DO_24
M_DATA B25	AP13	SB_DO_25
M_DATA B26	AL12	SB_DO_26
M_DATA B27	AL12	SB_DO_27
M_DATA B28	AL28	SB_DO_28
M_DATA B29	AL29	SB_DO_29
M_DATA B30	AP12	SB_DO_30
M_DATA B31	AR28	SB_DO_31
M_DATA B32	AR29	SB_DO_32
M_DATA B33	AL28	SB_DO_33
M_DATA B34	AL29	SB_DO_34
M_DATA B35	AP28	SB_DO_35
M_DATA B36	AP29	SB_DO_36
M_DATA B37	AM28	SB_DO_37
M_DATA B38	AM29	SB_DO_38
M_DATA B39	AP31	SB_DO_39
M_DATA B40	AP35	SB_DO_40
M_DATA B41	AP34	SB_DO_41
M_DATA B42	AP34	SB_DO_42
M_DATA B43	AR32	SB_DO_43
M_DATA B44	AR31	SB_DO_44
M_DATA B45	AR32	SB_DO_45
M_DATA B46	AR34	SB_DO_46
M_DATA B47	AM32	SB_DO_47
M_DATA B48	AM31	SB_DO_48
M_DATA B49	AL35	SB_DO_49
M_DATA B50	AL32	SB_DO_50
M_DATA B51	AM34	SB_DO_51
M_DATA B52	AL31	SB_DO_52
M_DATA B53	AM35	SB_DO_53
M_DATA B54	AL34	SB_DO_54
M_DATA B55	AH35	SB_DO_55
M_DATA B56	AE34	SB_DO_56
M_DATA B57	AE34	SB_DO_57
M_DATA B58	AJ35	SB_DO_58
M_DATA B59	AJ34	SB_DO_59
M_DATA B60	AF33	SB_DO_60
M_DATA B61	AF35	SB_DO_61
M_DATA B62		SB_DO_62
M_DATA B63		SB_DO_63
M_DQS B P0	AH7	SB_DQS_0
M_DQS B P1	AM8	SB_DQS_1
M_DQS B P2	AR8	SB_DQS_2
M_DQS B P3	AN13	SB_DQS_3
M_DQS B P4	AN29	SB_DQS_4
M_DQS B P5	AP33	SB_DQS_5
M_DQS B P6	AL33	SB_DQS_6
M_DQS B P7	AG35	SB_DQS_7
M_DQS B N0	AH6	SB_DQS#_0
M_DQS B N1	AL8	SB_DQS#_1
M_DQS B N2	AP8	SB_DQS#_2
M_DQS B N3	AV22	SB_DQS#_3
M_DQS B N4	AN26	SB_DQS#_4
M_DQS B N5	AR33	SB_DQS#_5
M_DQS B N6	AM33	SB_DQS#_6
M_DQS B N7	AG34	SB_DQS#_7

CPU1D

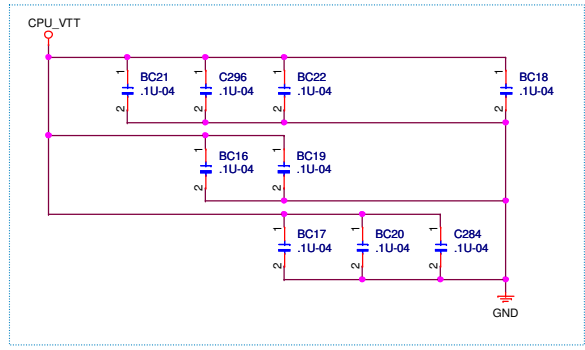
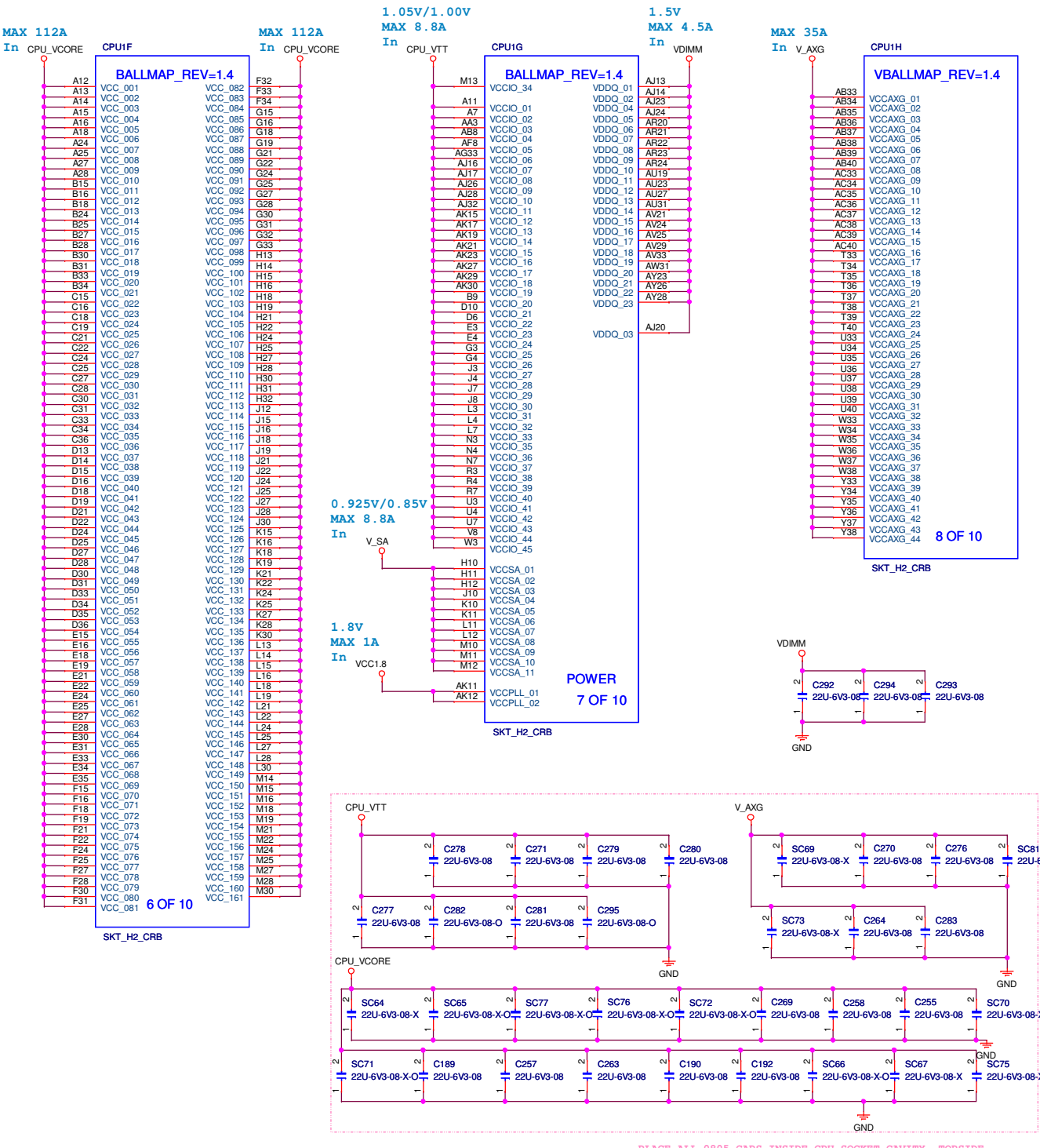
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Q0.0		S
Q0.1		S
Q0.2		S
Q0.3		S
Q0.4		S
Q0.5		S
Q0.6		S
Q0.7		S
Q0.8		S
Q0.9		S
Q0.10		SB
Q0.11		SB
Q0.12		SB
Q0.13		SB
Q0.14		SB
Q0.15		SB
Q0.16		
Q0.17		
Q0.18		S
Q0.19		S
Q0.20		SA
Q0.21		
Q0.22		
Q0.23		S
Q0.24		S
Q0.25		S
Q0.26		
Q0.27		
Q0.28		SB
Q0.29		SB
Q0.30		SB
Q0.31		SB
Q0.32		
Q0.33		
Q0.34		
Q0.35		SB
Q0.36		SB
Q0.37		SB
Q0.38		SB
Q0.39		SB
Q0.40		
Q0.41		
Q0.42		SB
Q0.43		SB
Q0.44		SB
Q0.45		SB
Q0.46		
Q0.47		
Q0.48		
Q0.49		S
Q0.50		SB
Q0.51		S
Q0.52		SB
Q0.53		SB
Q0.54		S
Q0.55		S
Q0.56		SB
Q0.57		
Q0.58		
Q0.59		
Q0.60		
Q0.61		
Q0.62		
Q0.63		
Q0S_0		SB
Q0S_1		SB
Q0S_2		
Q0S_3		
Q0S_4		
Q0S_5		SB_EC
Q0S_6		SB_EC
Q0S_7		SB_EC
Q0S#_0		SB_EC
Q0S#_1		SB_EC
Q0S#_2		SB_EC
Q0S#_3		SB_EC
Q0S#_4		SB_EC
Q0S#_5		SB_EC
Q0S#_6		SB_EC
Q0S#_7		SB_EC
Q0S#_8		DDR
Q0S#_9		4 OF

DDR3 CH.B

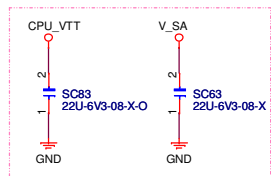
DDR_1

4 OF 10

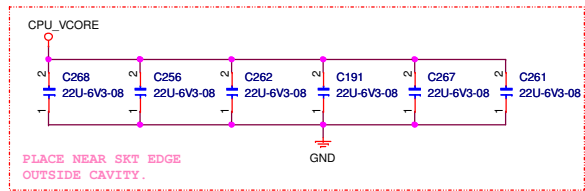
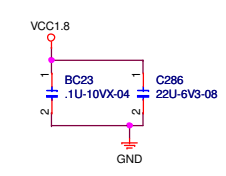
SKT_H2_CRB



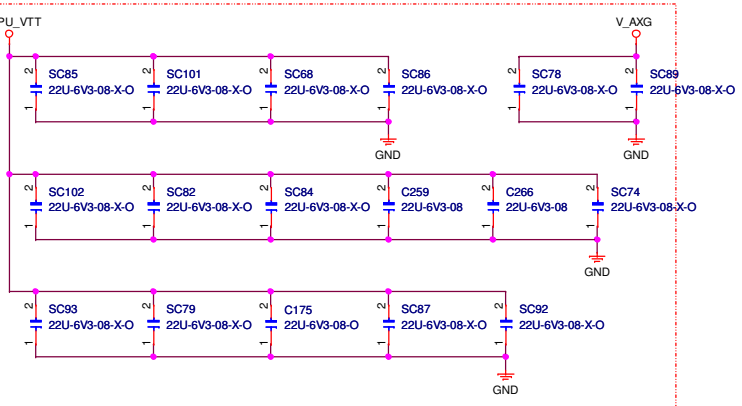
DECOUPLING & STITCHING CAPS.



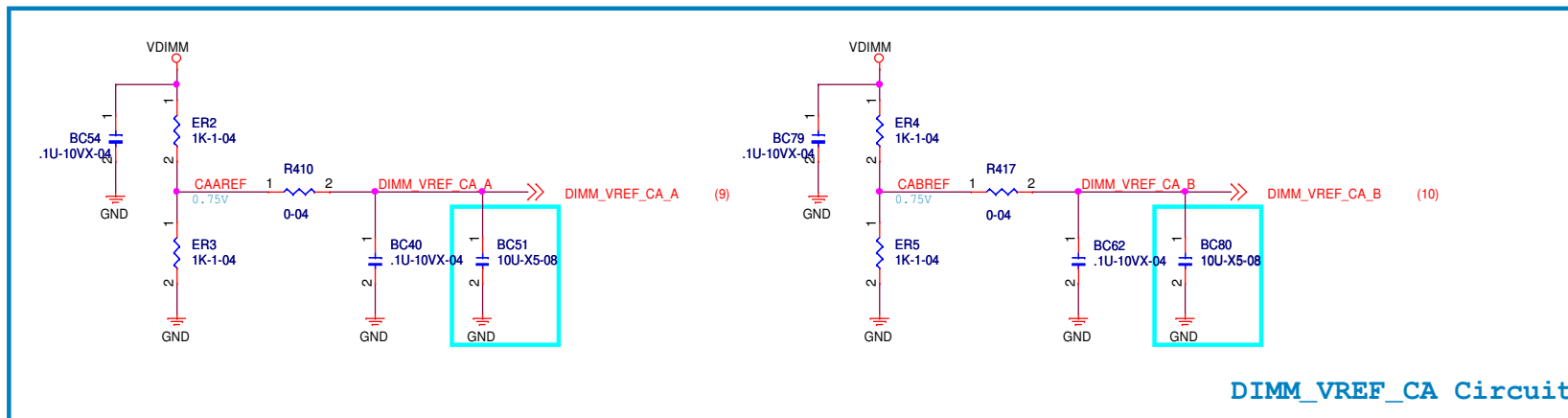
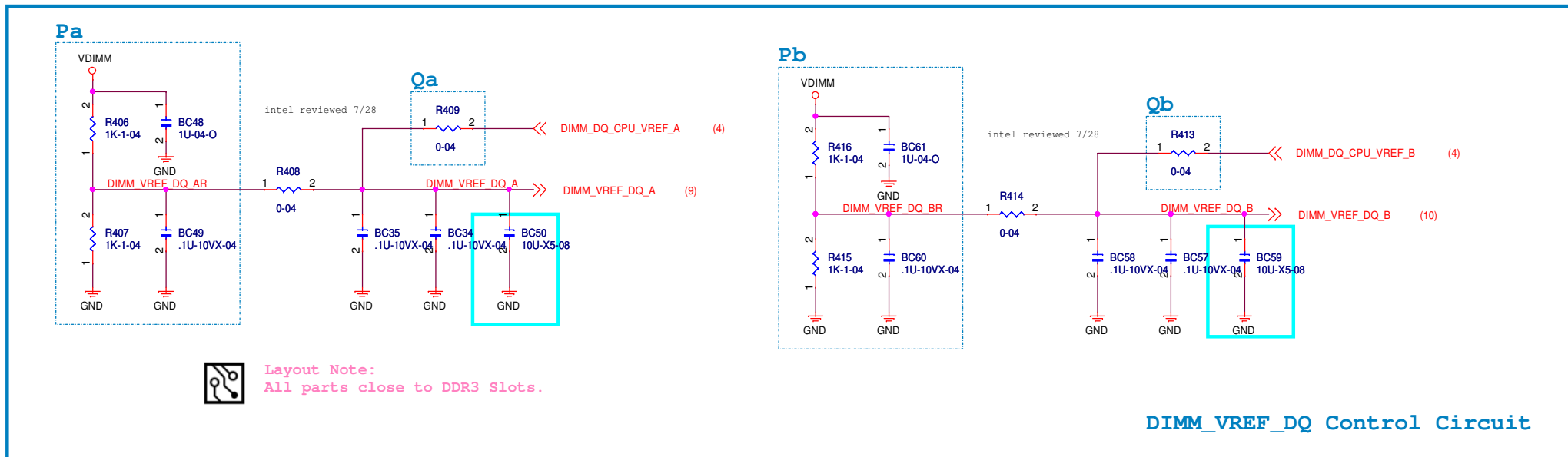
PLACE NEAR SKT EDGE OUTSIDE CAVITY.

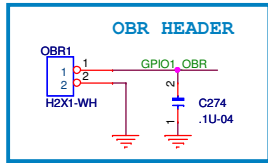
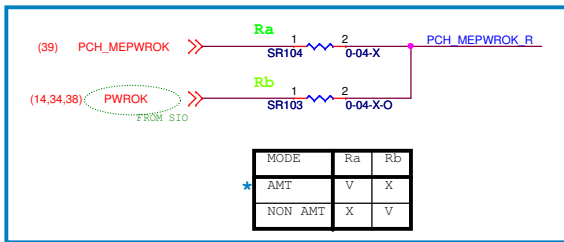


PLACE NEAR SKT EDGE OUTSIDE CAVITY.



PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY, BACKSIDE.



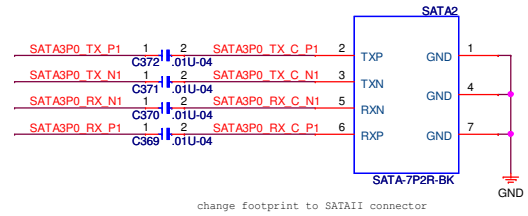
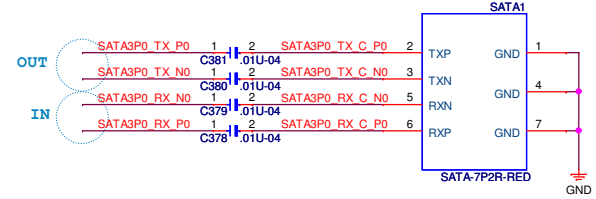
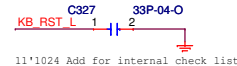
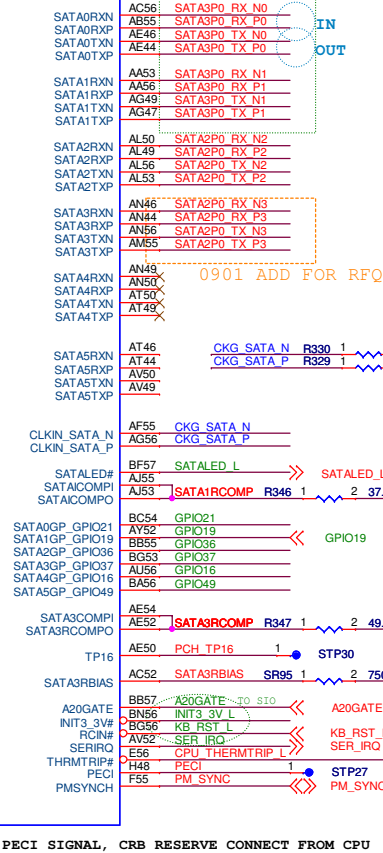
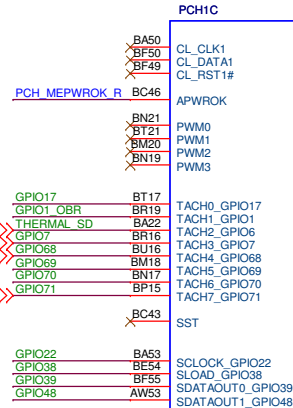
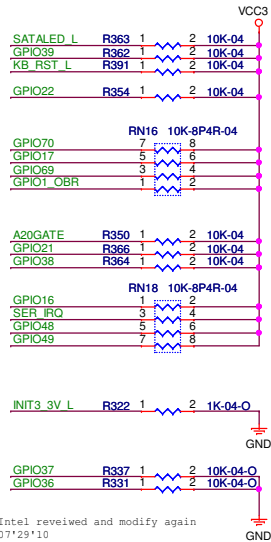


(12,34) THERMAL_SD

(12) GPIO7

(12) GPIO68

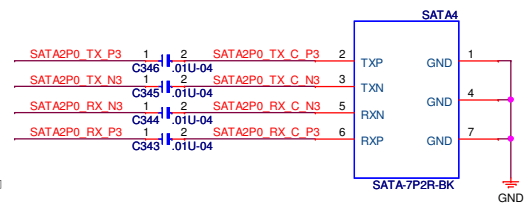
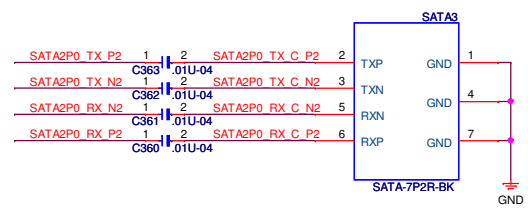
(12) GPIO71



Layout Note:

SATA3.0 4.5/7.5/20 in 90 Ω $\pm 17.5\%$

SATA2.0 4.5/7.5/15 in 90 Ω $\pm 17.5\%$

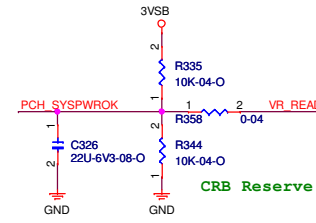
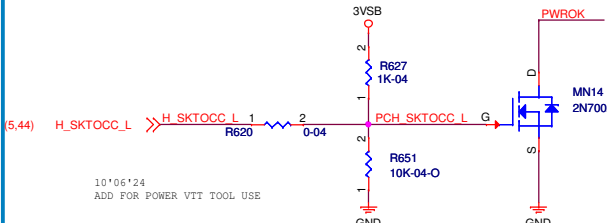
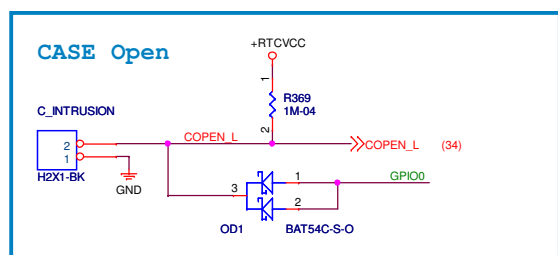
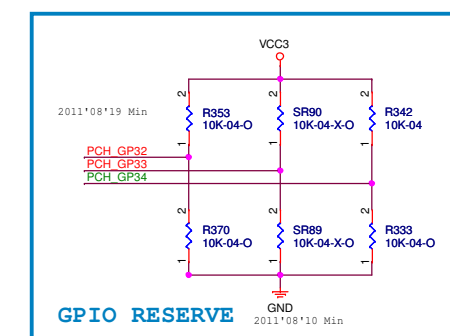
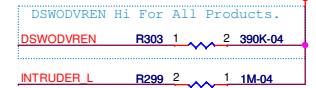
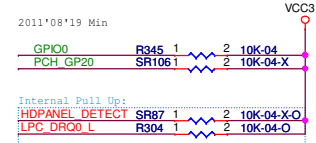
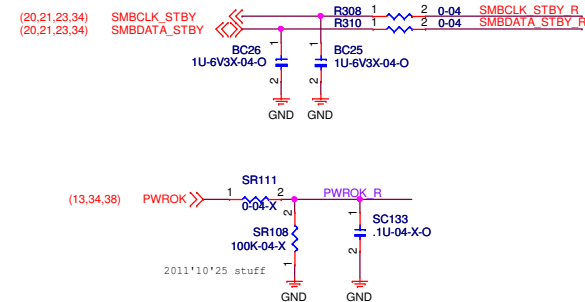
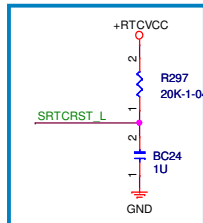
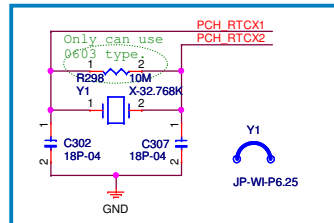
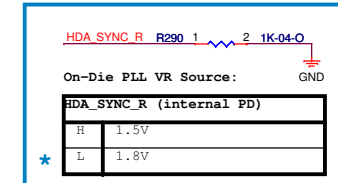
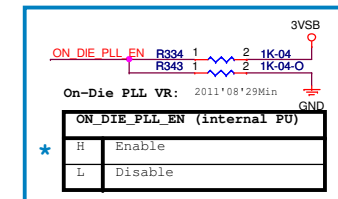
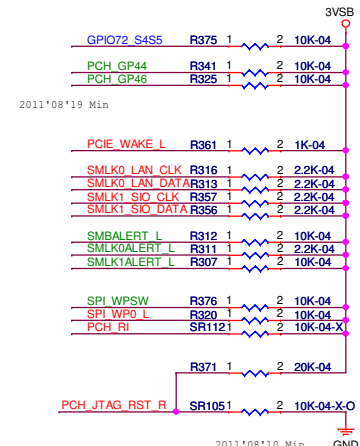
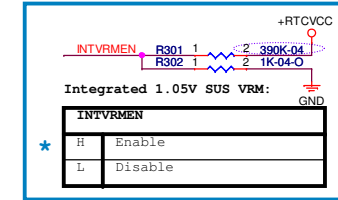
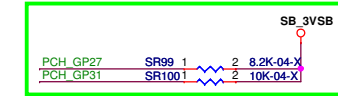
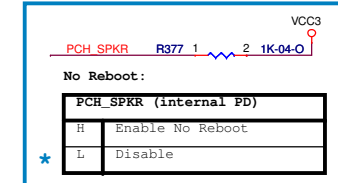
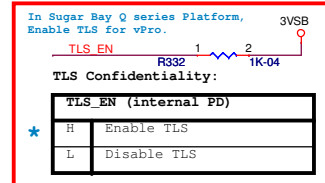
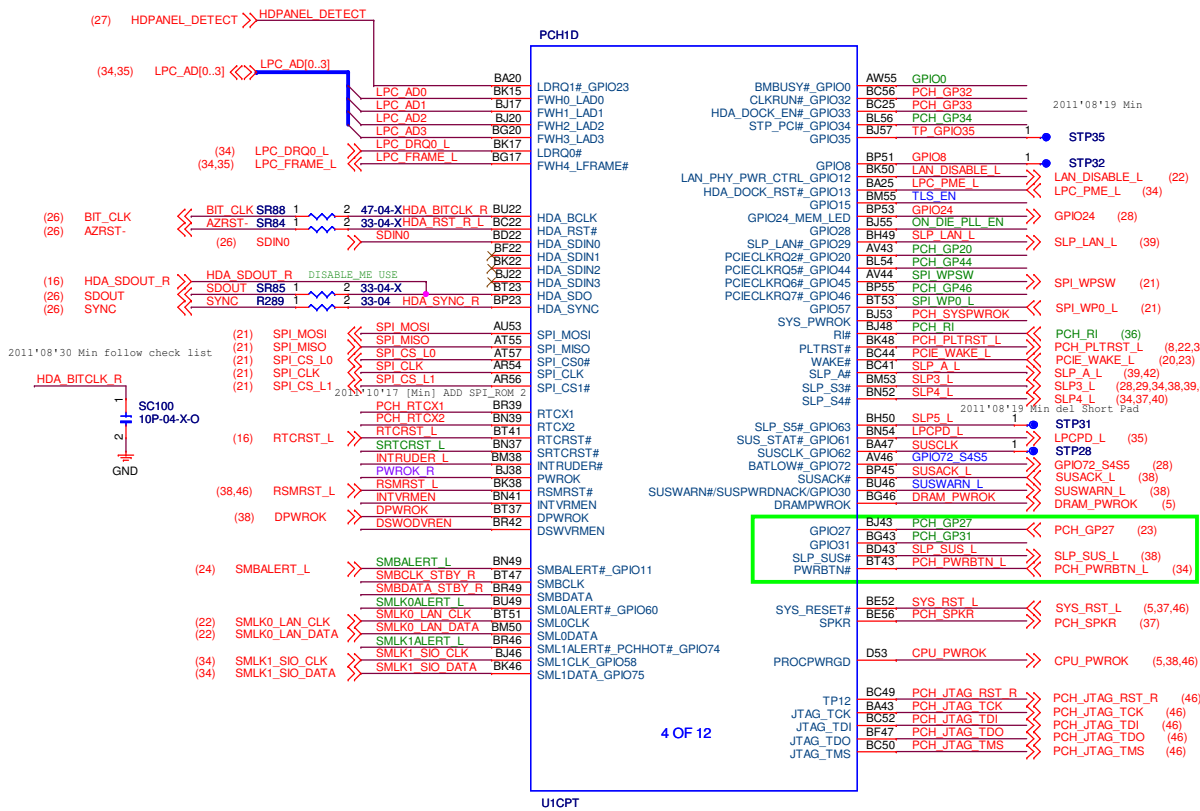


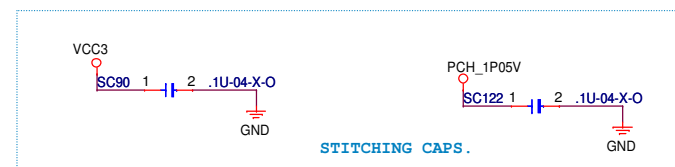
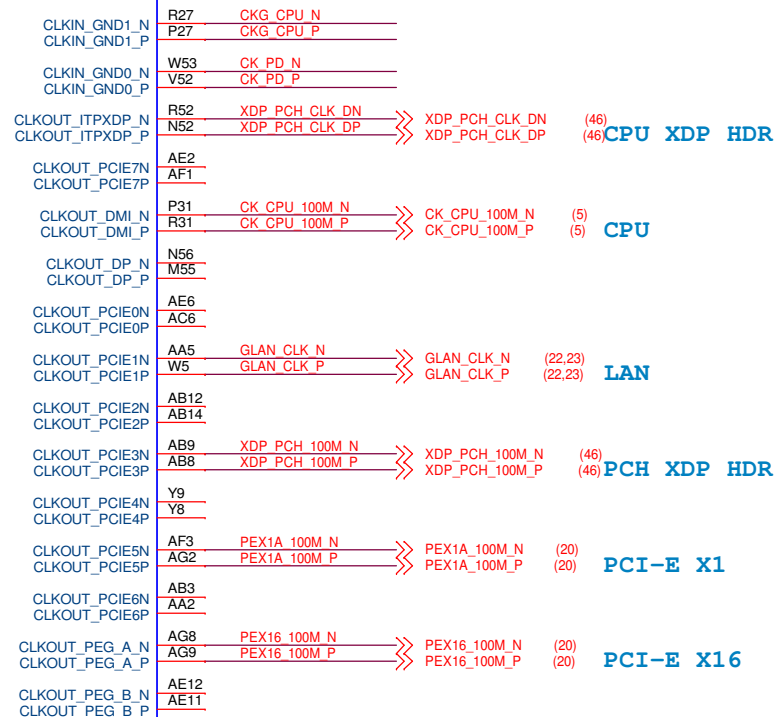
ECS Elitegroup Computer Systems

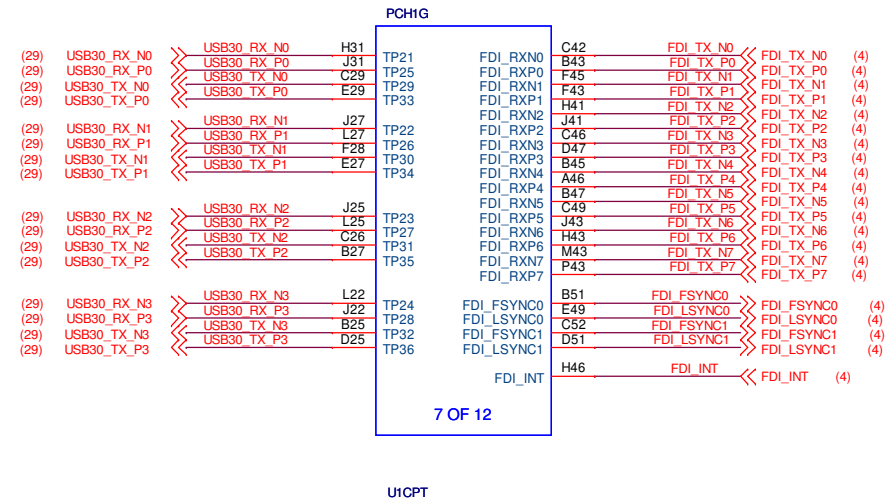
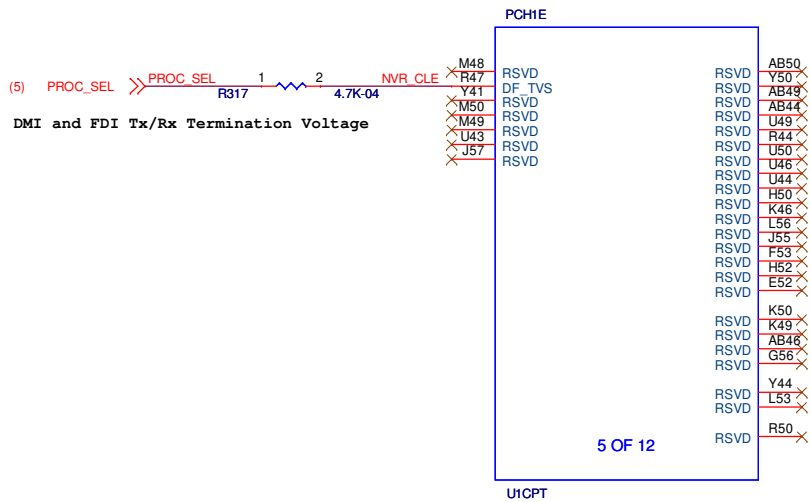
Title PCH - SATA, SATA CONN, OBR

Size Custom Document Number B75H2-AD Rev 1.0

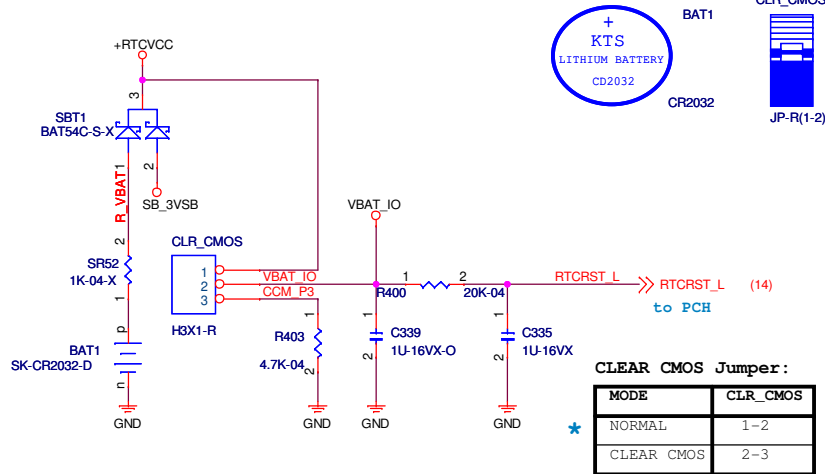
Date: Wednesday, April 18, 2012 Sheet 13 of 49



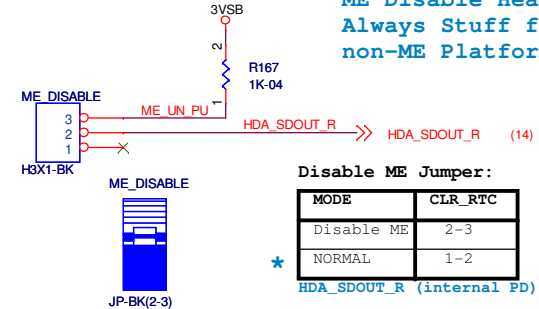




CLR_CMOS



ME Disable Header,
Always Stuff for ME or
non-ME Platform.



Elitegroup Computer Systems

Title **PCH - USB3.0/FDI, CLR_CMOS**

Size B Document Number **B75H2-AD**

Rev 1.0

Date: Wednesday, April 18, 2012 Sheet 16 of 49

Port-B: DVII

Port-C: DP

Port-D: DP

[M 1007] PORTB CHANGE TO CONNECT TO DVI-I
PORT D CHANGE TO CONNECT TO DP

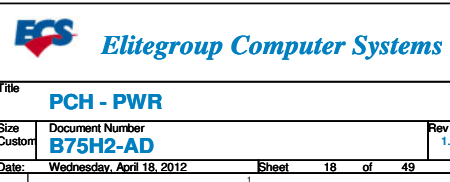
6 of 12

Port C Detected(Internal PD):
Port C is Detected when High,
Port C is not Detect when Low.
Port D Detected(Internal PD):
Port D is Detected when High,
Port D is not Detect when Low.
Port B Detected(Internal PD):
Port B is Detected when High,
Port B is not Detect when Low.

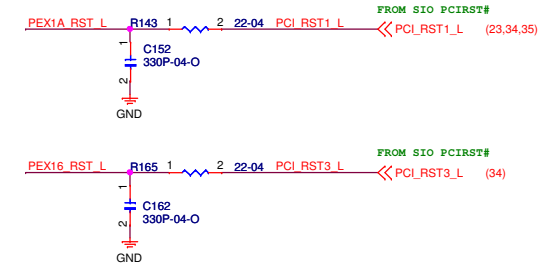
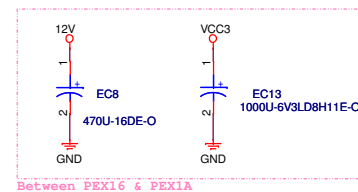
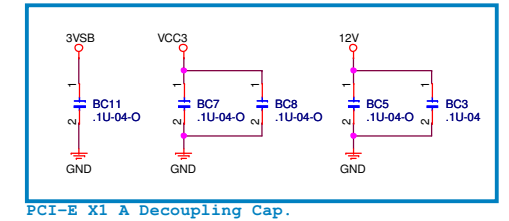
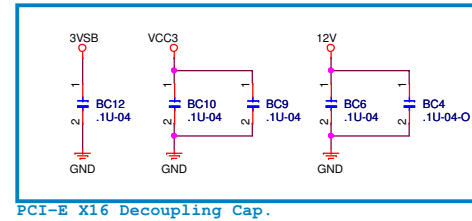
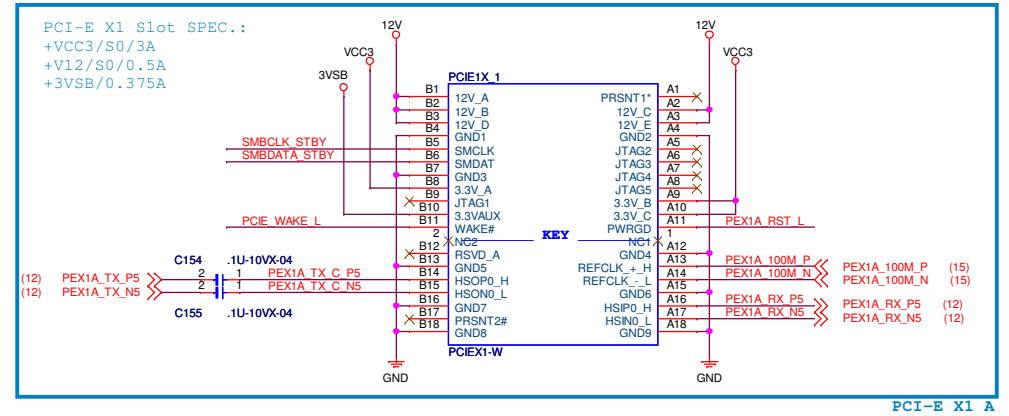
[M 1007] PORTB CHANGE TO CONNECT TO DVI-I
PORT D CHANGE TO CONNECT TO DP



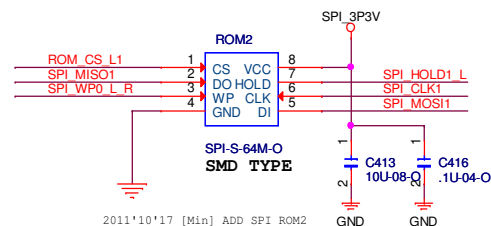
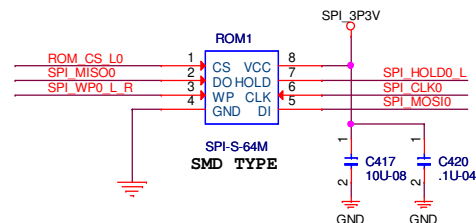
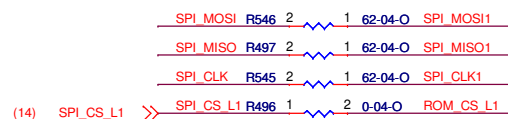
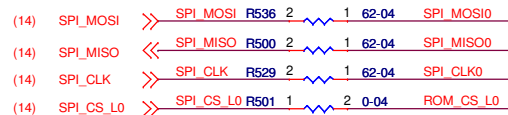
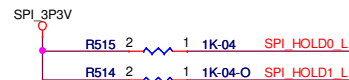
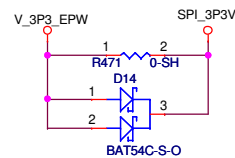
Title		
PCH - DISPLAY/VGA		
Size	Document Number	Rev
Custom	B75H2-AD	1.0.
Date:	Wednesday, April 18, 2012	Sheet 17 of 49



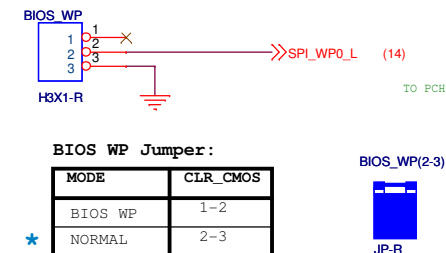
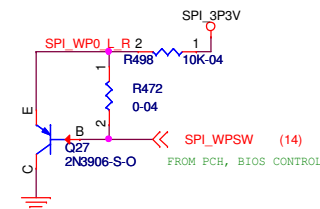
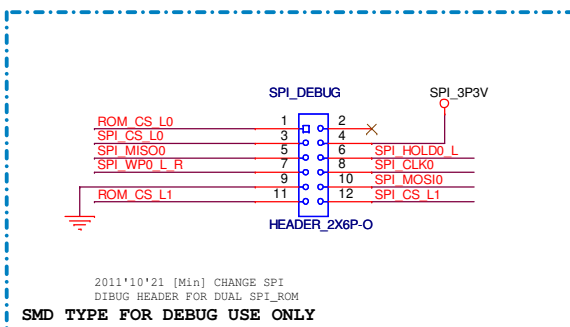
PCI-E X16 Slot SPEC.:
+VCC3/S0/3A
+V12/S0/5.5A
+3VSB/0.375A



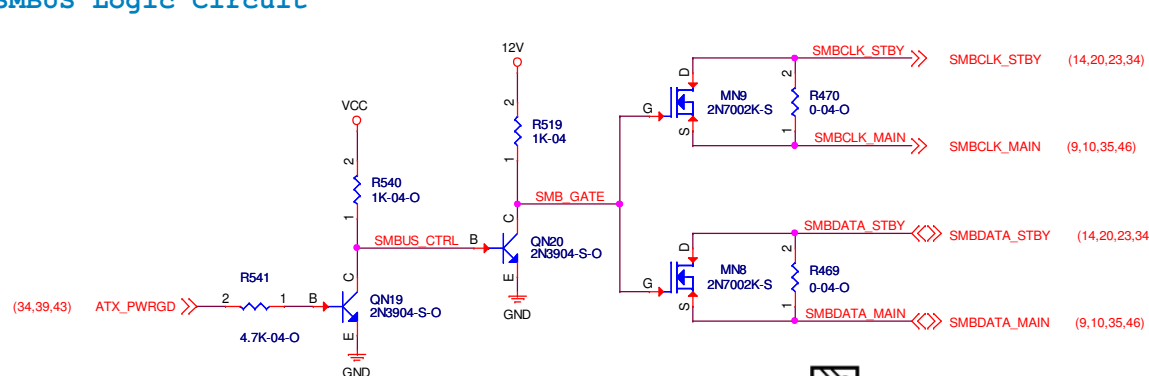
SPI ROM Circuit



2011'10'17 [Min] ADD SPI ROM2



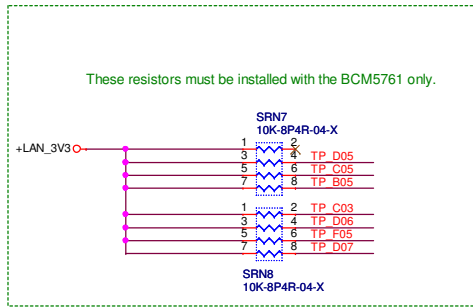
SMBUS Logic Circuit



Layout Note:
SMBUS Trace Max 21500MILS

ECS Elitegroup Computer Systems

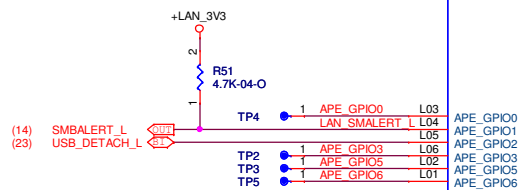
Title			SPI ROM, SMBUS
Size	Document Number	Rev	
Custom	B75H2-AD	1.0.	
Date:	Wednesday, April 18, 2012	Sheet	21 of 49



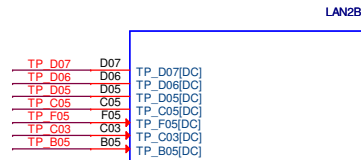
Ruart_mode should be installed to enable the debug UART function when the BCM5754 is used.



Rd8_pd must be installed with the BCM5761 only.

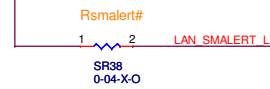
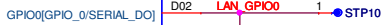
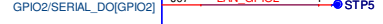
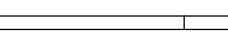
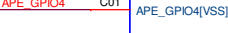
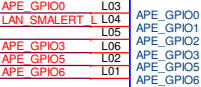
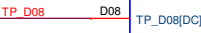
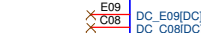


Rvss_5754 must be installed when the BCM5754 is used.

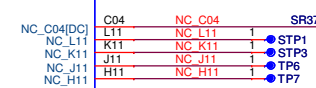


BCM5761/BCM5754

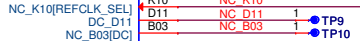
Name - 5761
Name - 5754 unless different
[Name] - 5754 only



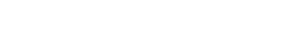
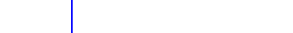
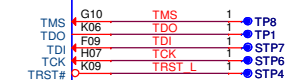
Rsmalert# should be installed when the BCM5754 ASF doorbell function is used.



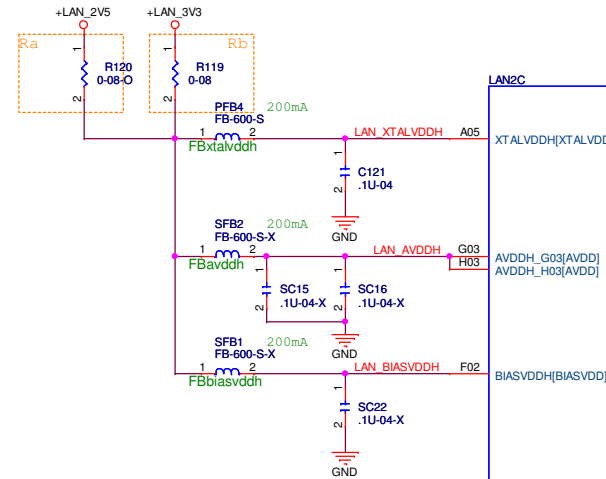
For Energy Detection function use only for 5761E use



Rrefcksel must not be installed with the BCM5761, but may be installed with the BCM5754

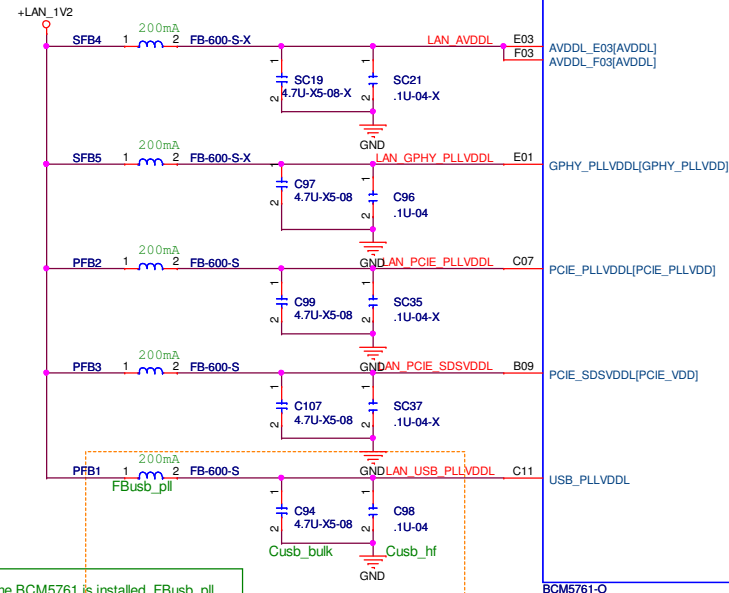


	5754	5761
Ra	V	X
Rb	X	V



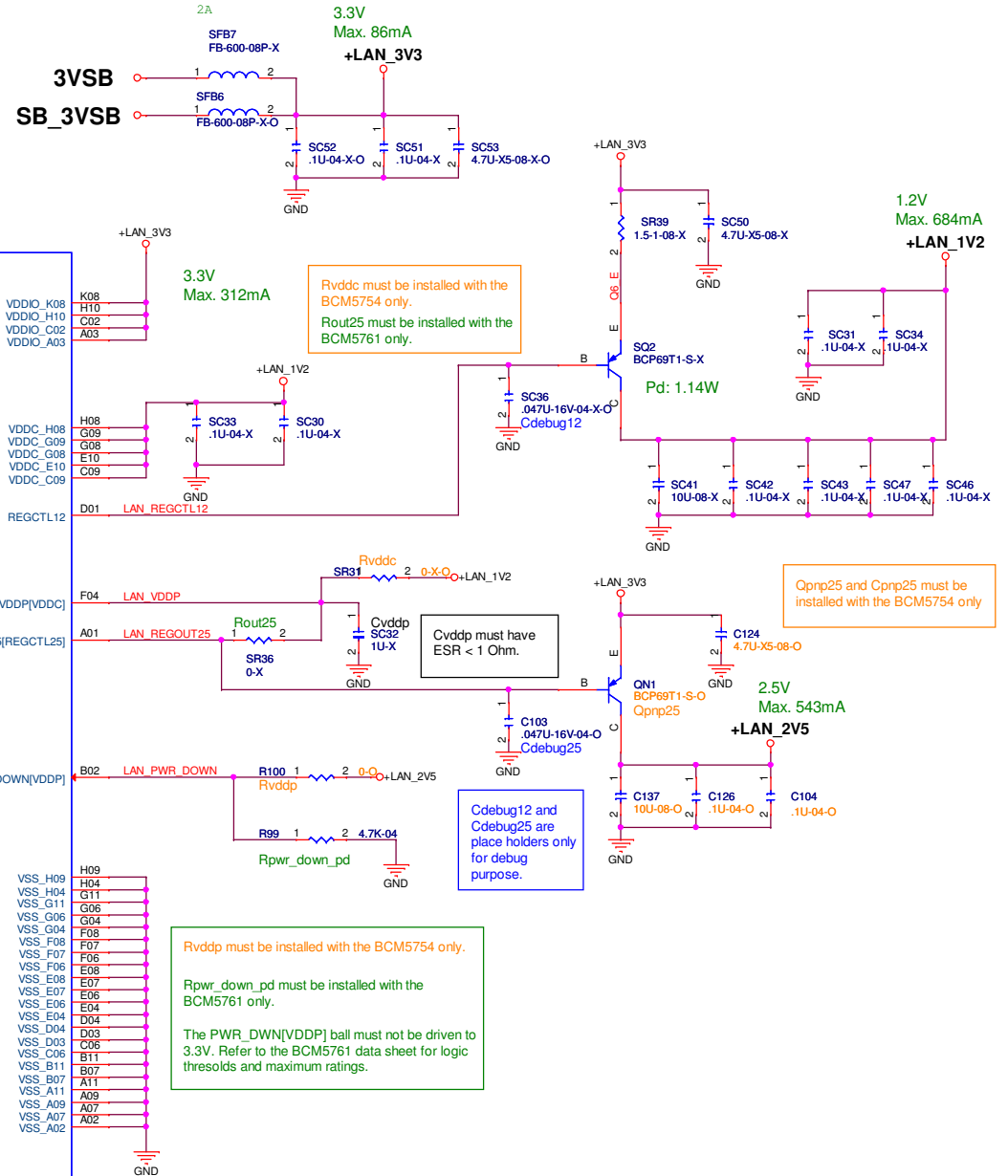
BCM5761/BCM5754

Name - 5761
Name - 5754 unless different
[Name] - 5754 only



If the BCM5761 is installed, FBusb_pll, Cusb_bulk, and Cusb_hf must be laid out even if the USB interface is not used since the USB PLL may provide an alternate clock source internal to the BCM5761.

If the BCM5754 is installed, FBusb_pll, Cusb_bulk, and Cusb_hf may be uninstalled.

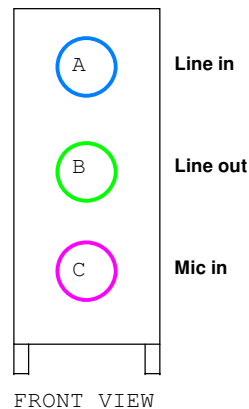
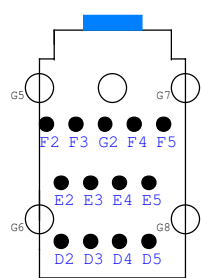
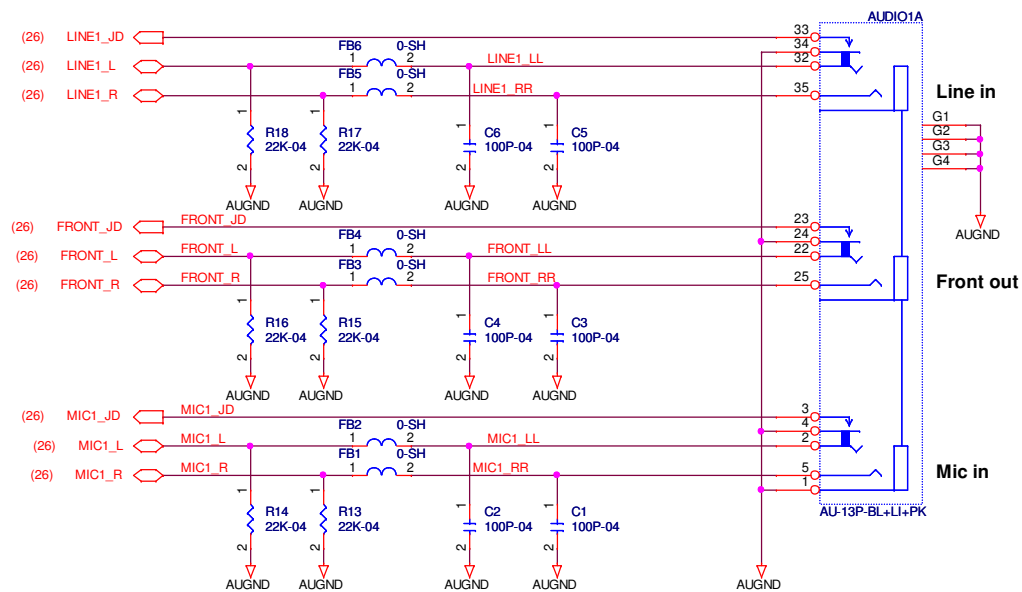


Rvddc must be installed with the BCM5754 only.
Rout25 must be installed with the BCM5761 only.

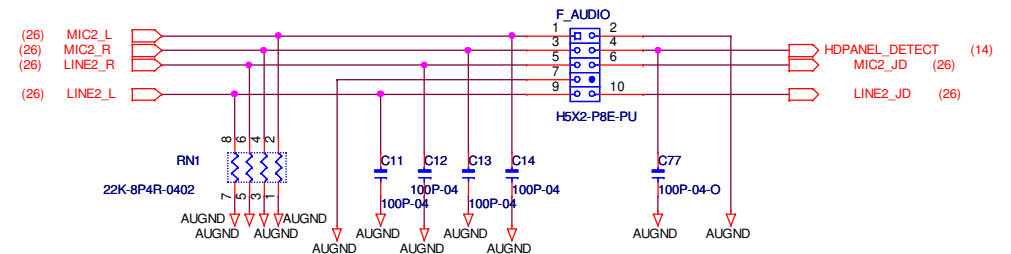
Cvddp must have ESR < 1 Ohm.

Cdebug12 and Cdebug25 are place holders only for debug purpose.

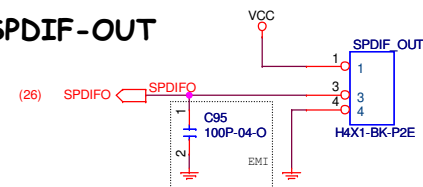
REAR-AUDIO



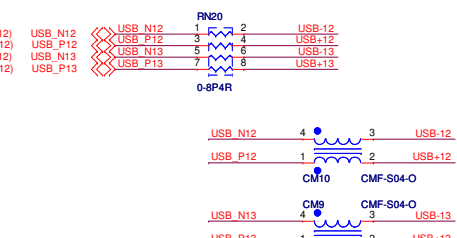
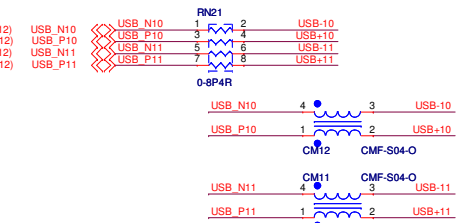
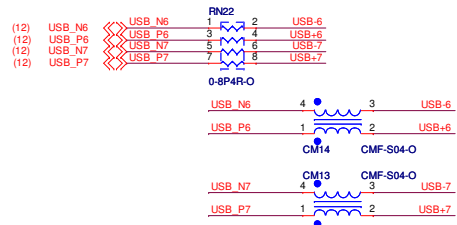
FRONT-AUDIO



SPDIF-OUT

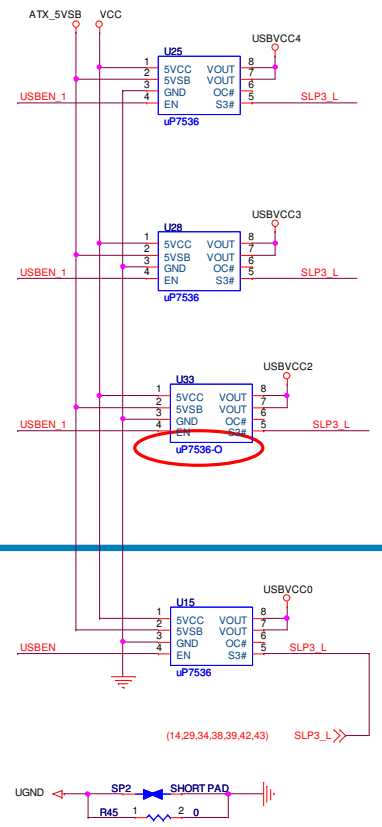
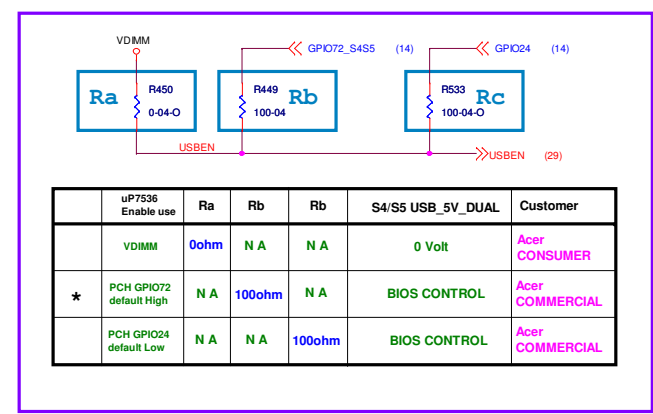
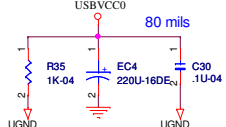
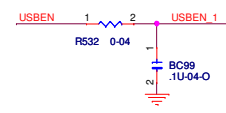
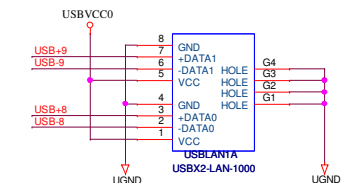
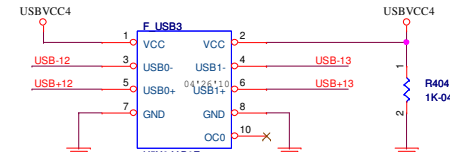
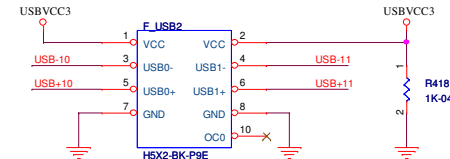
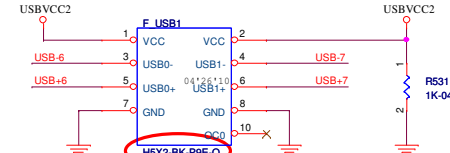
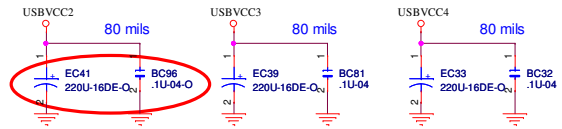
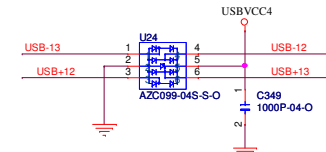
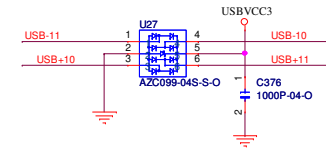
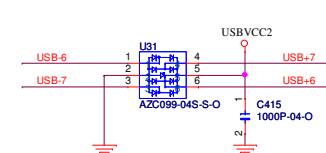
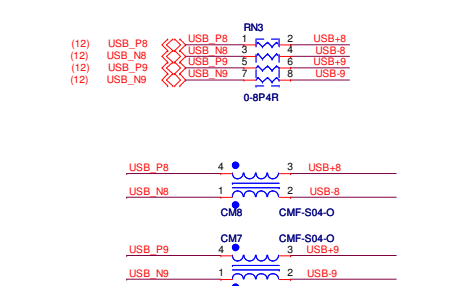


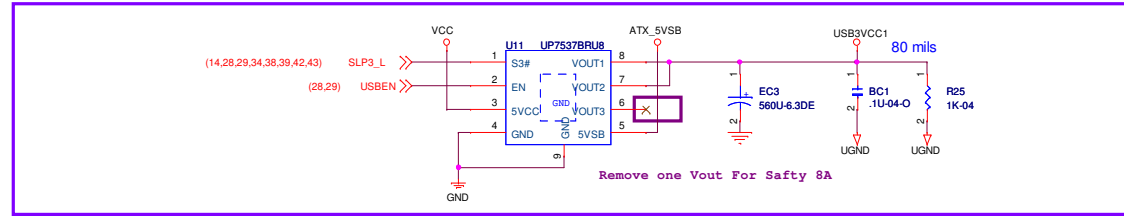
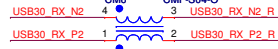
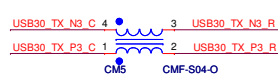
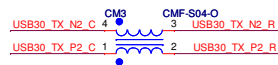
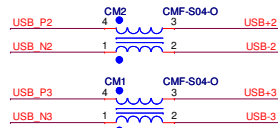
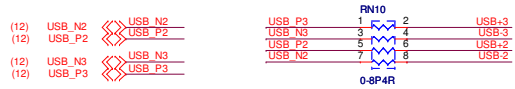
AUDIO ALC662 Connector (PANEL)	
Title	Document Number B75H2-AD
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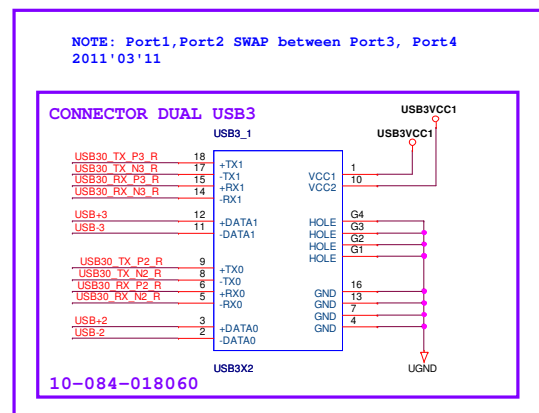
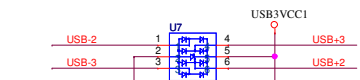
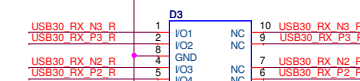
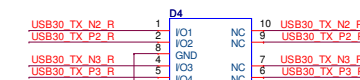
FRONT PANEL USB2.0 HEADER

REAR PANEL USB2.0 CONNECTOR



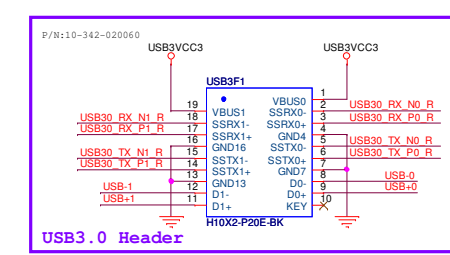
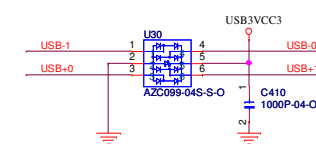
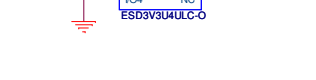
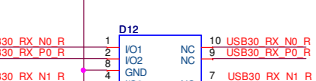
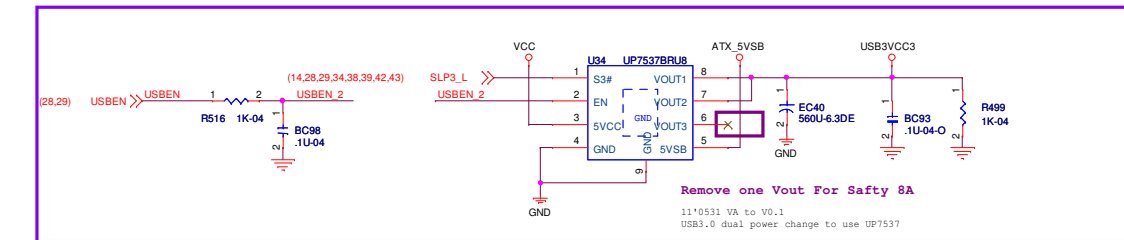
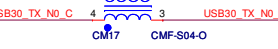
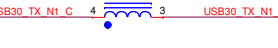
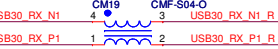
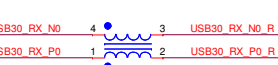
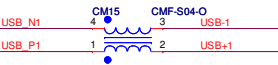
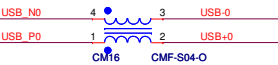


USB3 ESD COMPONENTS



REAR PANEL USB3.0 CONNECTOR

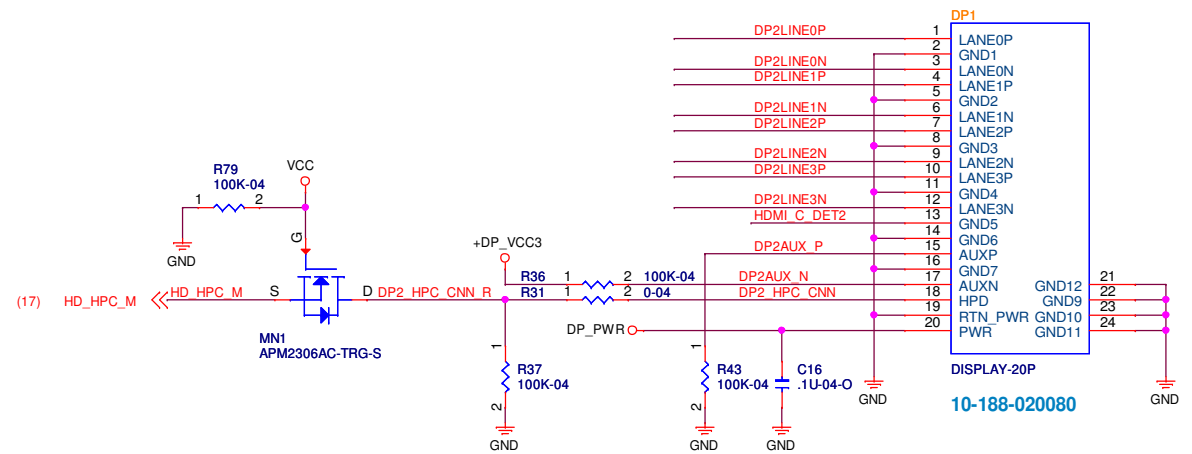
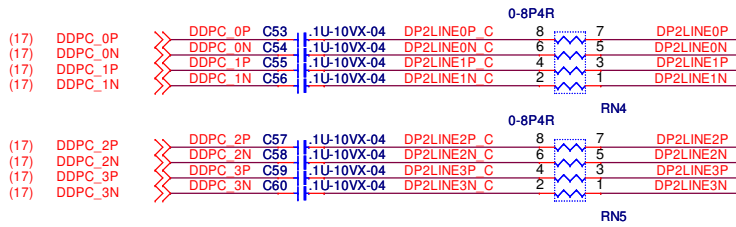
FRONT PANEL USB3.0 HEADER



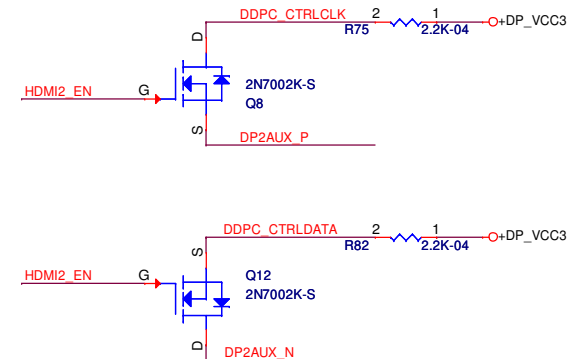
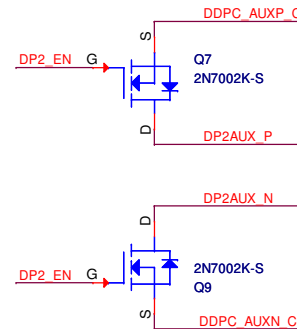
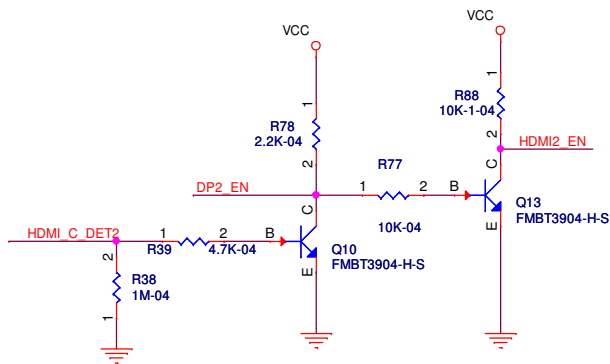
USB3 ESD COMPONENTS

(17) DDPC_CTRLDATA >> DDPC_CTRLDATA
(17) DDPC_CTRLCLK >> DDPC_CTRLCLK

(17) DDPC_AUXP >> DDPC_AUXP C44 :1U-10VX-04 DDPC_AUXP_C
(17) DDPC_AUXN >> DDPC_AUXN C41 :1U-10VX-04 DDPC_AUXN_C

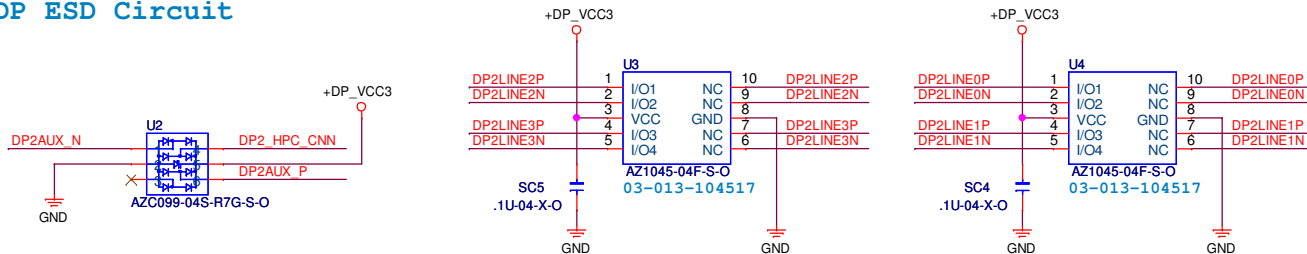


10-188-020080



SUPPORT DP TO HDMI/DVI DONGLE

DP ESD Circuit



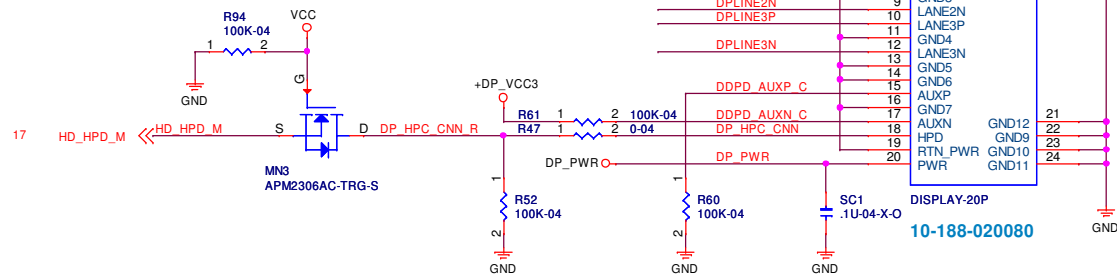
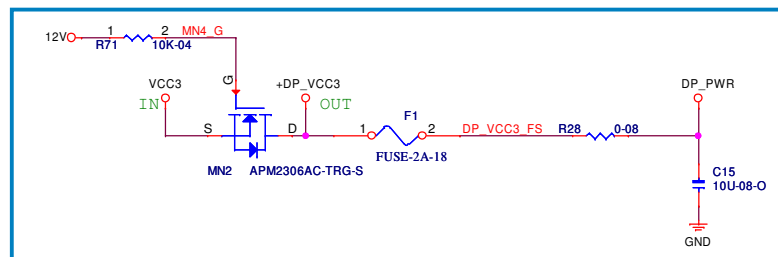
ECS Elitegroup Computer Systems

Title		DISPLAY PORT1
Size	Document Number	B75H2-AD
Custom		Rev 1.0
Date:	Wednesday, April 18, 2012	Sheet 30 of 49

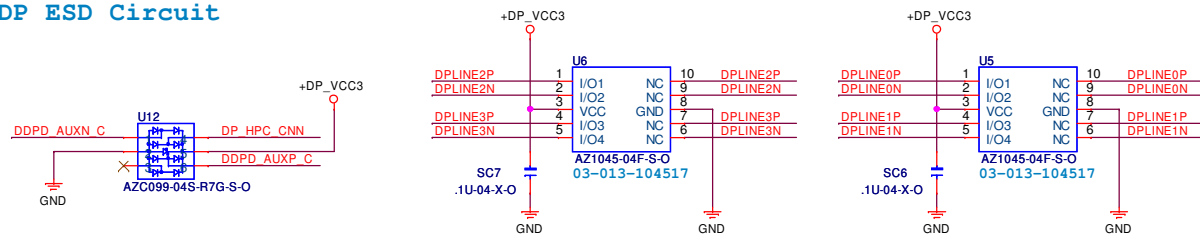
DDPD_AUXP >> DDPD_AUXP C80 >> 1U-10VX-04 DDPD_AUXP C
DDPD_AUXN >> DDPD_AUXN C79 >> 1U-10VX-04 DDPD_AUXN C

DDPD_0P >> DDPD_0P C61 >> 1U-10VX-04 DPLINE0P C 8 7 DPLINE0P
DDPD_0N >> DDPD_0N C62 >> 1U-10VX-04 DPLINE0N C 6 5 DPLINE0N
DDPD_1P >> DDPD_1P C63 >> 1U-10VX-04 DPLINE1P C 4 3 DPLINE1P
DDPD_1N >> DDPD_1N C64 >> 1U-10VX-04 DPLINE1N C 2 1 DPLINE1N
RN6

DDPD_2P >> DDPD_2P C65 >> 1U-10VX-04 DPLINE2P C 8 7 DPLINE2P
DDPD_2N >> DDPD_2N C66 >> 1U-10VX-04 DPLINE2N C 6 5 DPLINE2N
DDPD_3P >> DDPD_3P C67 >> 1U-10VX-04 DPLINE3P C 4 3 DPLINE3P
DDPD_3N >> DDPD_3N C68 >> 1U-10VX-04 DPLINE3N C 2 1 DPLINE3N
RN7

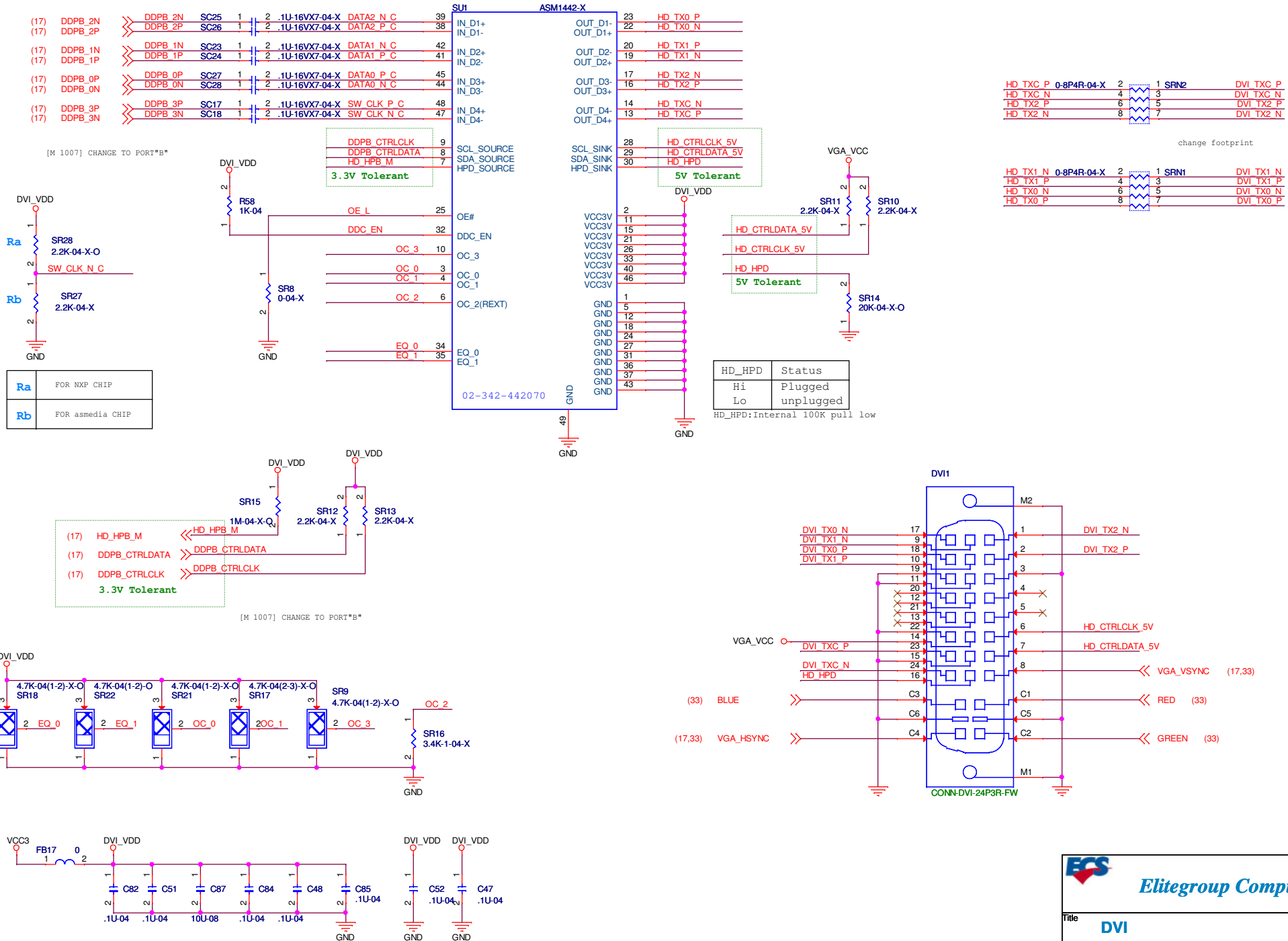


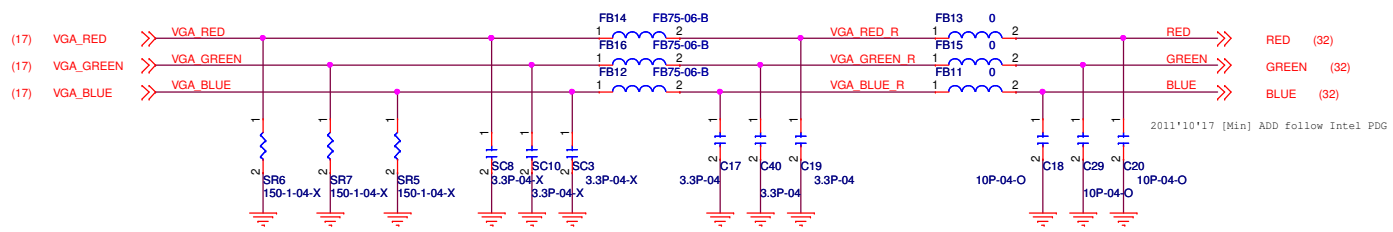
DP ESD Circuit



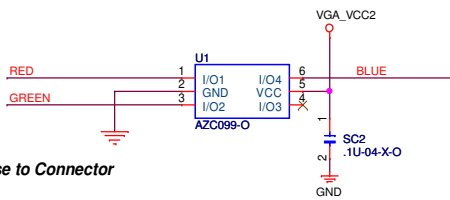
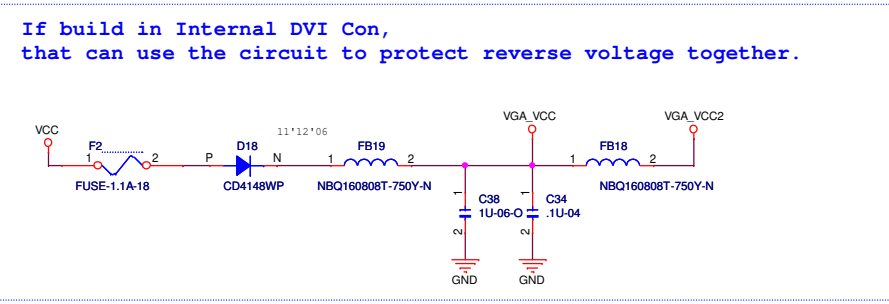
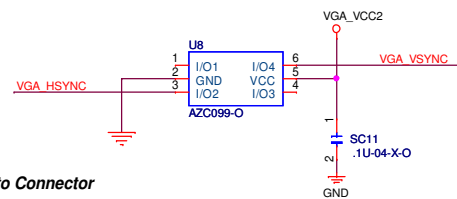
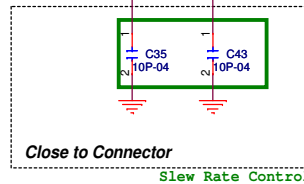
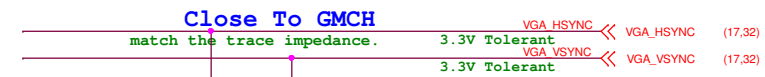
Title		
DISPLAY PORT2		
Size	Document Number	Rev
Custom	B75H2-AD	1.0.
Date:	Wednesday, April 18, 2012	Sheet 31 of 49

Level Shifter





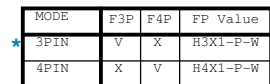
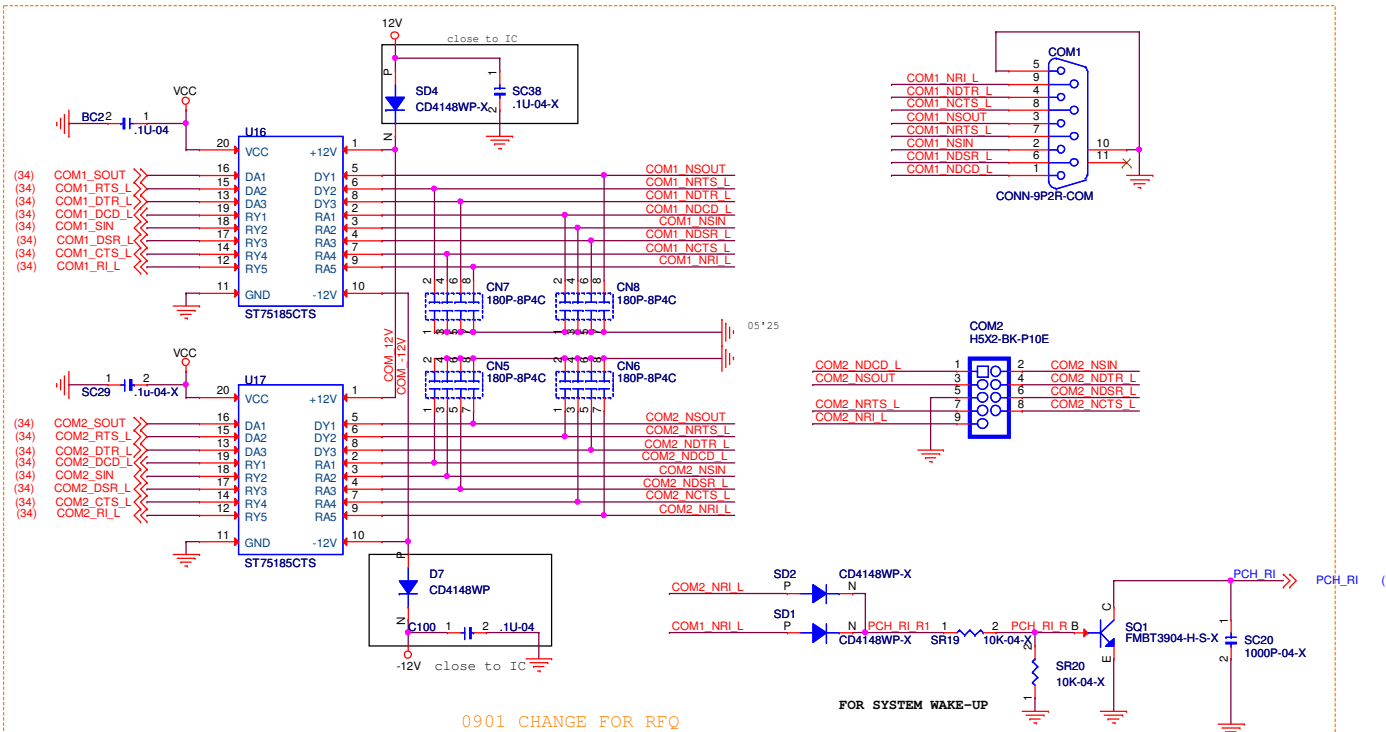
Close to Connector



LPT Header Circuit

TPM CHIP/Header Circuit

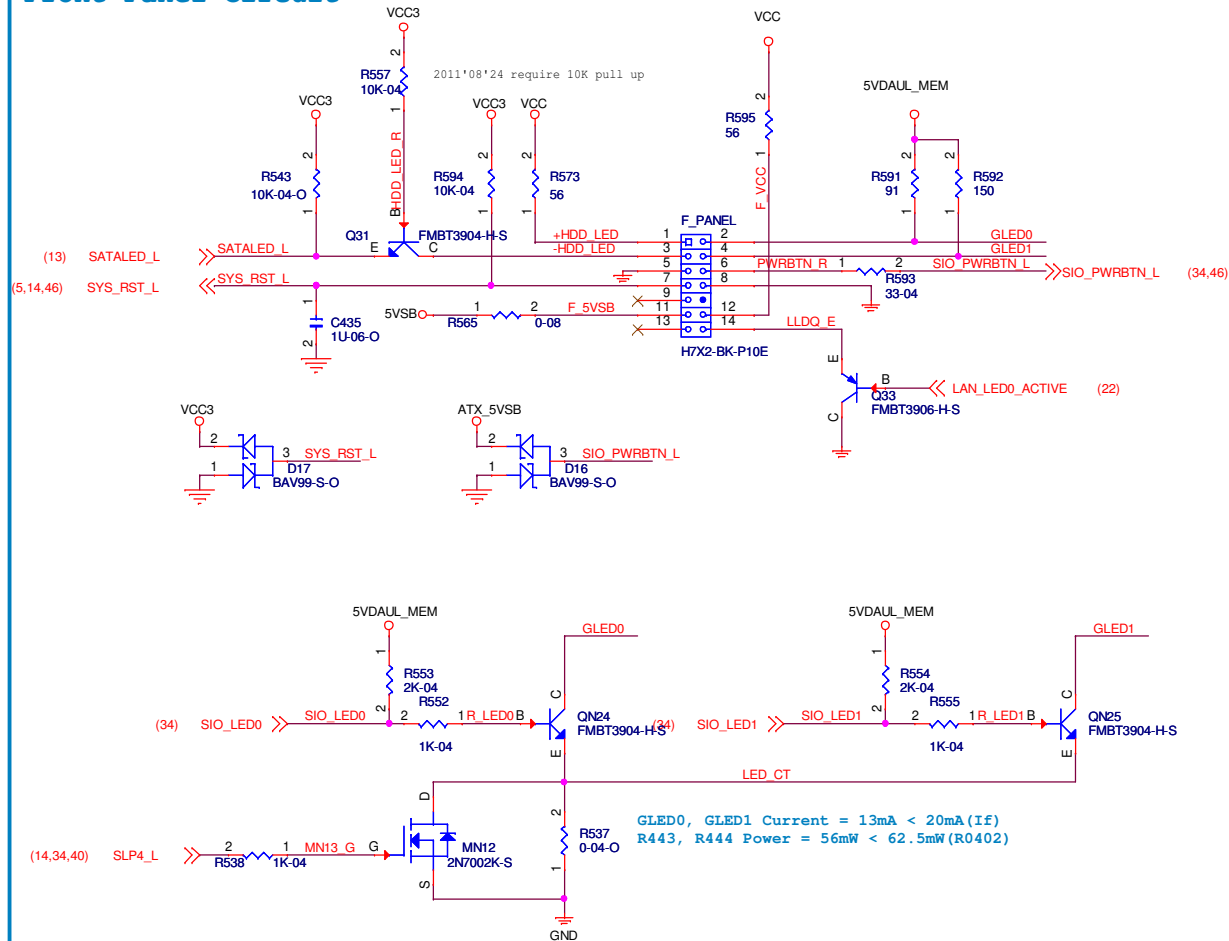
PS2-KB Circuit



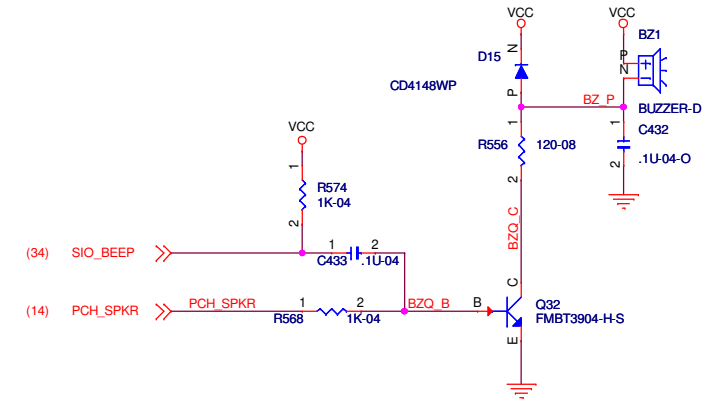
0901 CHANGE FOR RFQ

+ - terminal add short pad to ground for nonuse OP , 20110406

Front Panel Circuit



Buzzer Circuit



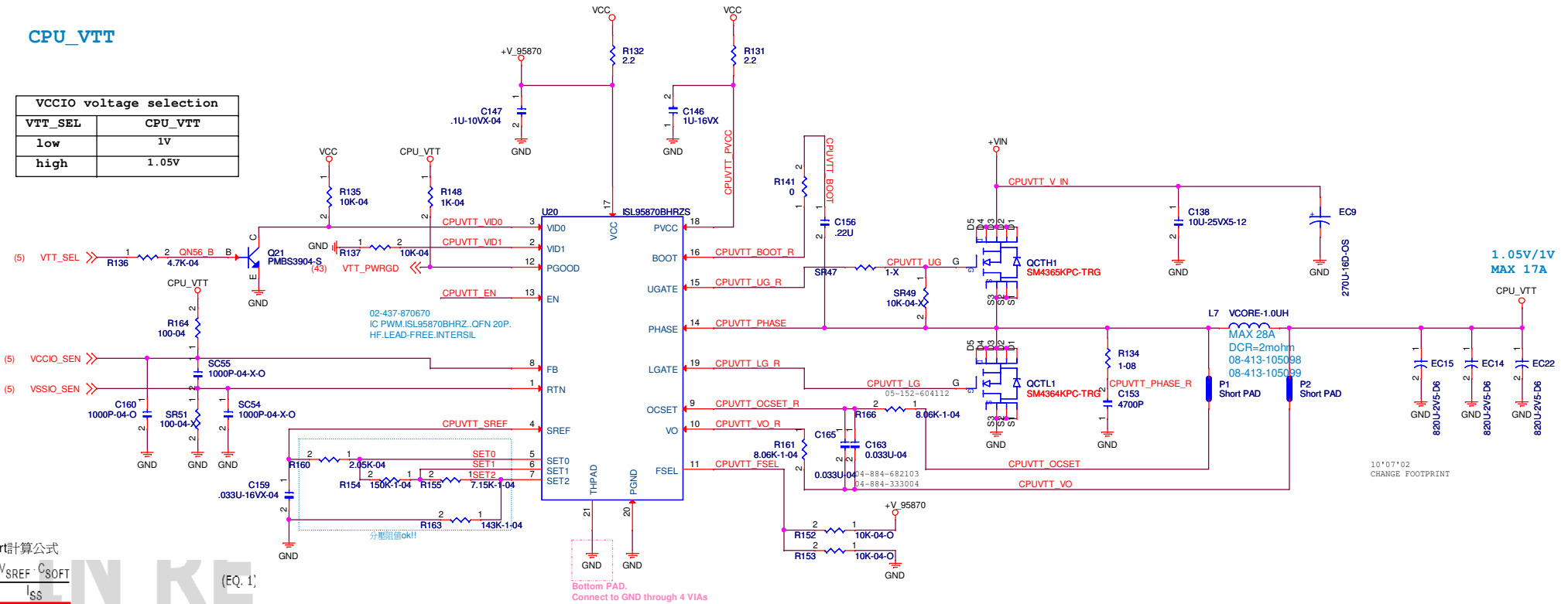
SLP4_L	High	Low
NCP1587DR2G	Enable	Disable

[illegible]

Layout Note:
SMVTTc close to U35 Pin4.
SMVTTcG are between Channel A & B.
SMVTTCh are between Channel A & CPU.

CPU_VTT

VCCIO voltage selection	
VTT_SEL	CPU_VTT
low	1V
high	1.05V



Soft-start計算公式

$$t_{SS} = \frac{V_{SREF} \cdot C_{SOFT}}{I_{SS}} \quad (EQ. 1)$$

Where:

- I_{SS} is the soft-start current source at the 20µA limit
- V_{SREF} is the buffered V_{REF} reference voltage

Vout計算公式

TABLE 2. ISL95870B VID TRUTH TABLE

VID STATE		RESULT	
VID1	VID0	CLOSE	VOUT
1	1	SW0	VOUT1
1	0	SW1	VOUT2
0	1	SW2	VOUT3
0	0	SW3	VOUT4

Equations 21, 22, 23 and 24 give the specific V_{SET} equations for the ISL95870B setpoint reference voltages.

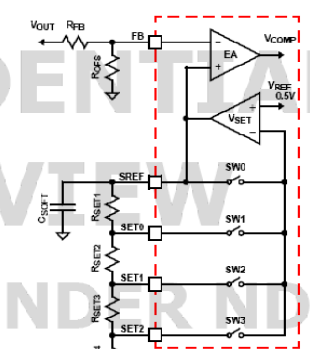
The ISL95870B V_{SET1} setpoint is written as Equation 21:
 $V_{SET1} = V_{REF}$ (EQ. 21)

The ISL95870B V_{SET2} setpoint is written as Equation 22:
 $V_{SET2} = V_{REF} \cdot \left(1 + \frac{R_{SET1}}{R_{SET2} + R_{SET3} + R_{SET4}}\right)$ (EQ. 22)

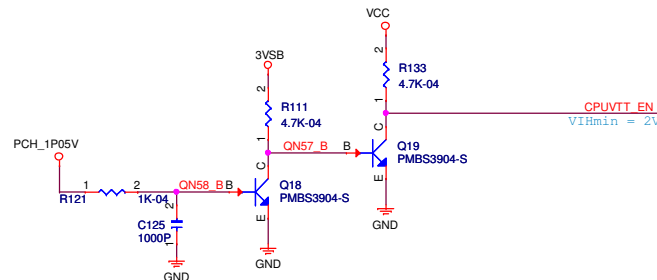
The ISL95870B V_{SET3} setpoint is written as Equation 23:
 $V_{SET3} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2}}{R_{SET3} + R_{SET4}}\right)$ (EQ. 23)

The ISL95870B V_{SET4} setpoint is written as Equation 24:
 $V_{SET4} = V_{REF} \cdot \left(1 + \frac{R_{SET1} + R_{SET2} + R_{SET3}}{R_{SET4}}\right)$ (EQ. 24)

FIGURE 10. ISL95870B VOLTAGE PROGRAMMING CIRCUIT



Frequency selection	
F (Hz)	FSEL
300K	Directly to GND
500K	Floating
600K	100K ohm to GND
1M	Pull-up to VCC



Default Stuffed:

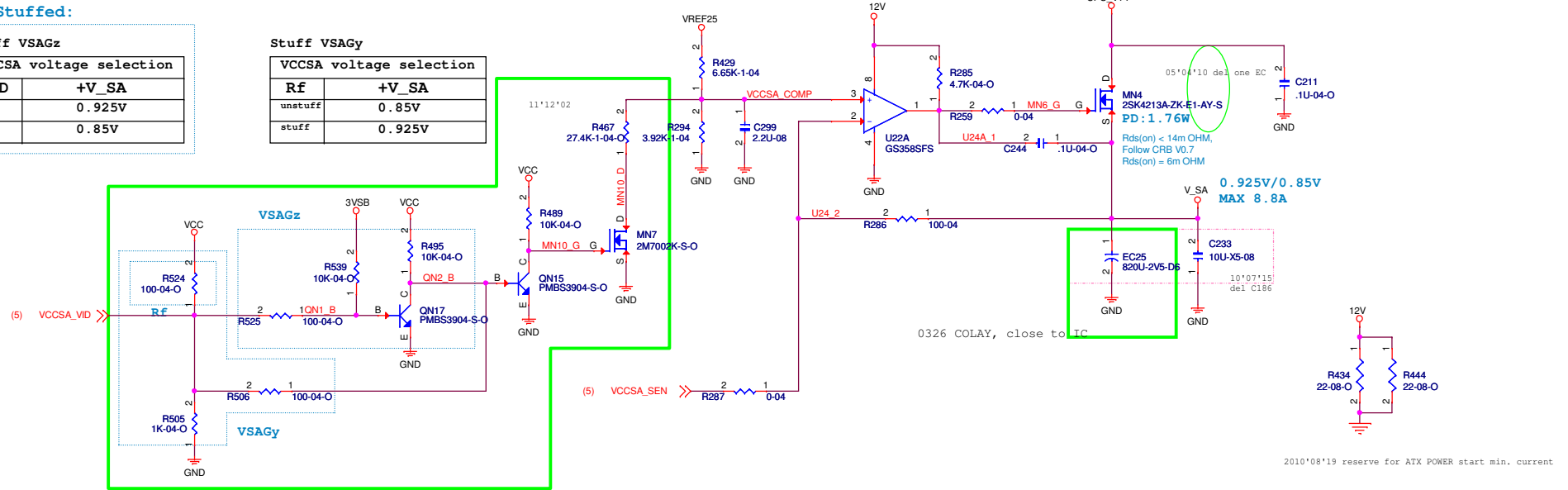
Stuff VSAGz

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

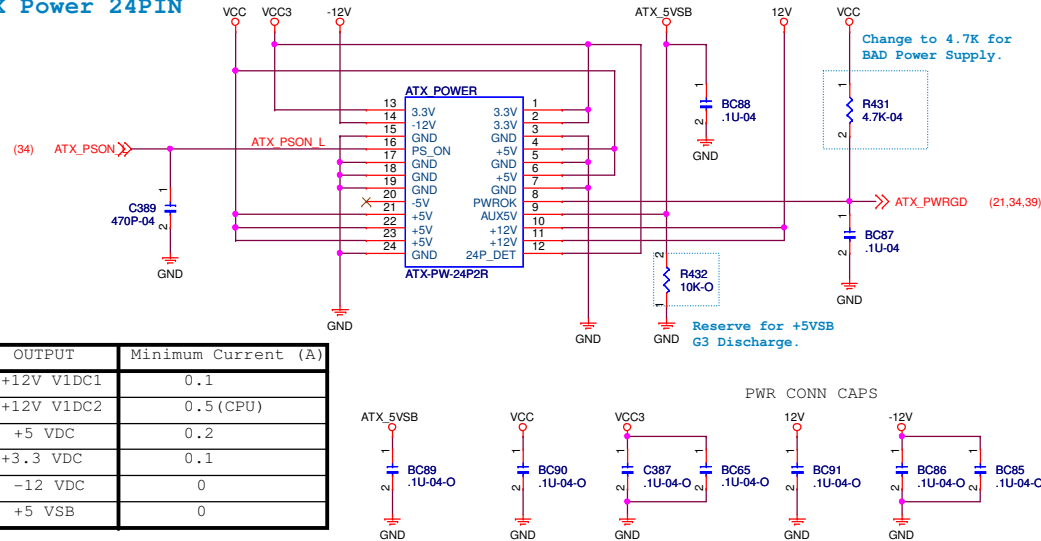
★

Stuff VSAGy

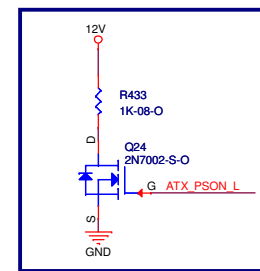
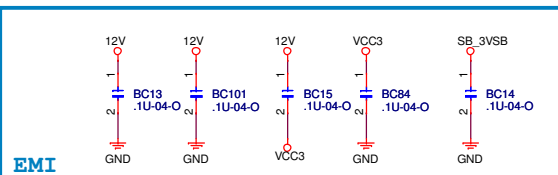
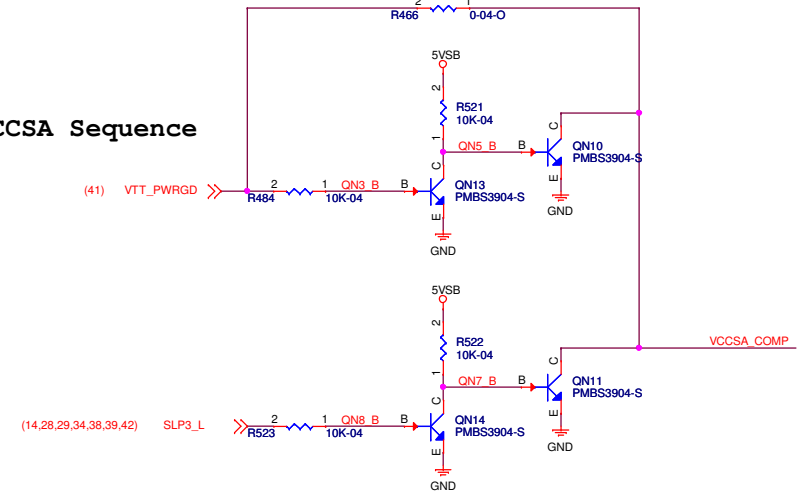
VCCSA voltage selection	
Rf	+V_SA
unstuff	0.85V
stuff	0.925V



ATX Power 24PIN



VCCSA Sequence



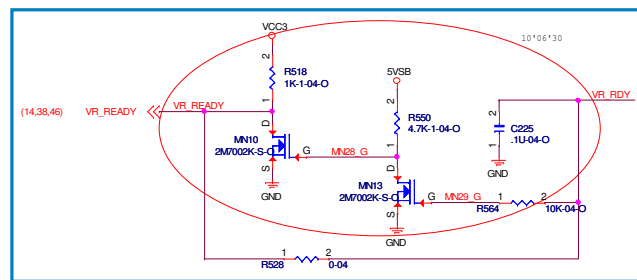
(38) VR_EN
(5) VR_SVID_ALERT_L
(5) VR_SVID_DATAOUT
(5) VR_SVID_CK
(5) VR_HOT_L

(5) VCC_SEN

(5) VSS_SEN

(5) VCCAXG_SEN

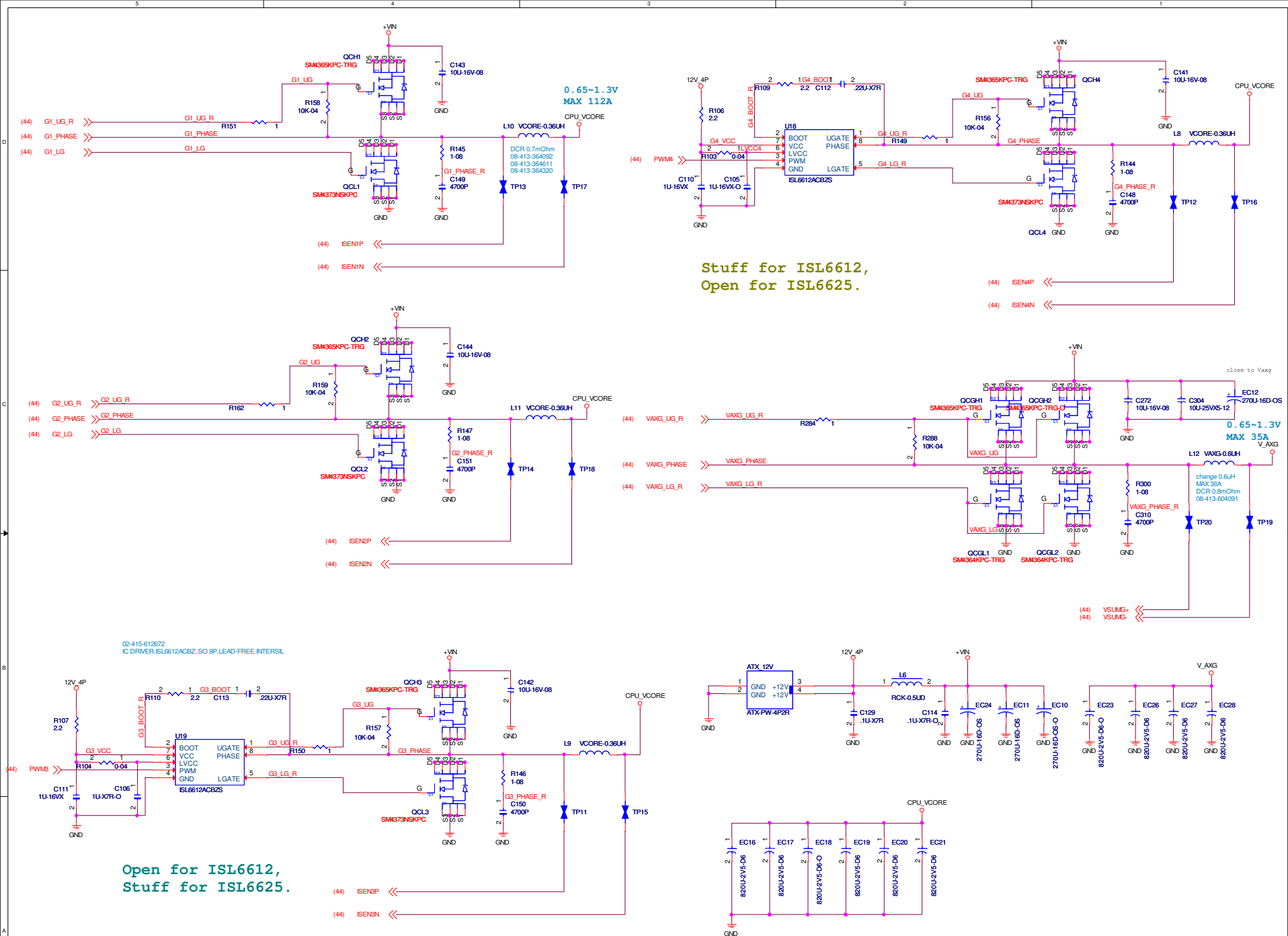
(5) VSSAXG_SEN

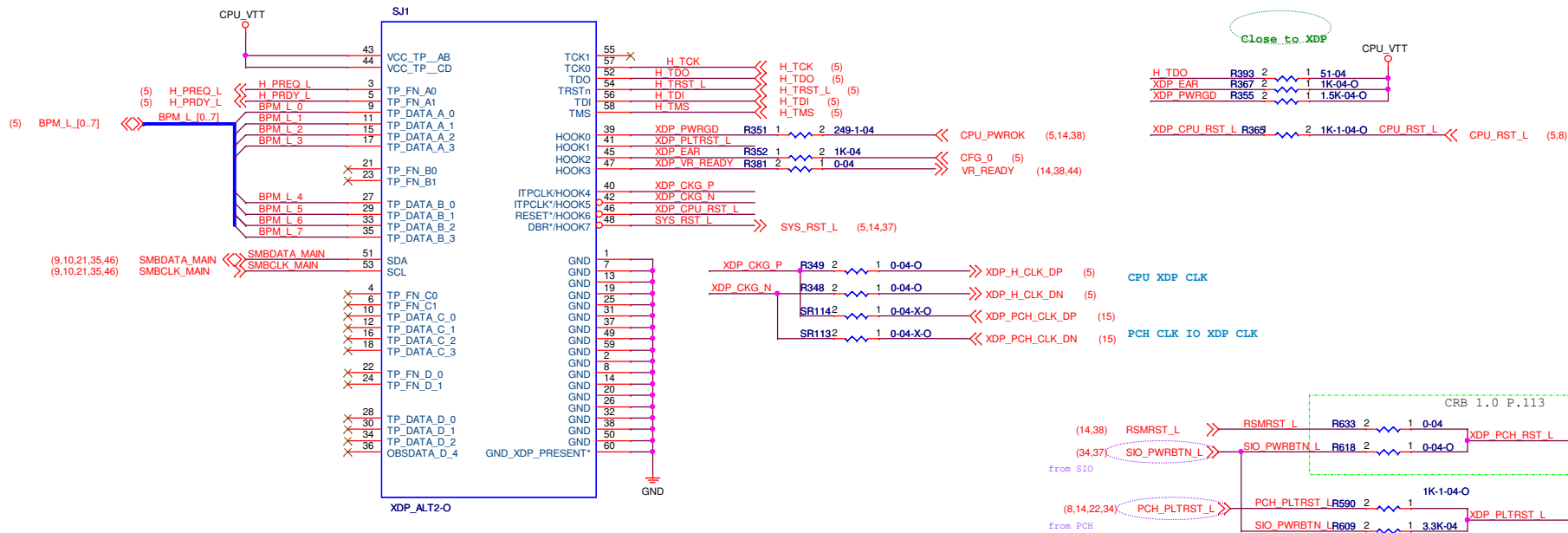


For VR_READY Power On Sequence

Bottom PAD
Connect to GND through 8 VtAs

Elitegroup Computer Systems





DESIGN NOTE:
PCH JTAG

DESIGN NOTE:
DEFENSIVE DESIGN

Title: **XDP**

Size: Custom

Document Number: **B75H2-AD**

Date: Wednesday, April 18, 2012

Rev: 1.0

Sheet 46 of 49

ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	+12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P
12V
+/-5%

Switching ISL6364 4+1 phases

Switching ISL95870B 1 phase

Switching NCP1587

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0
V_SM_VTT	1.0A_S0

Linear LM324

LDO APL5336

Linear LM324

Switching RT8015A

Linear LM324

Intel Ivy Bridge CPU		
VCCP	VTD 0.25~1.52V	85A(95W)
VAXG	VTD 0.25~1.52V	25A
VTT	1.05V(1V)	8.5A
VCC_SA	0.925V(0.85V)	8.8A
VCCPLL	1.8V	1A
VDDQ	1.5V	4.5A

Intel Panther Point (TDP 5.5W)		
V_PROC_IO	1.05V	1mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	1.6A
VccIO	1.05V	4.07A
VccADPLLA	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.02A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTERM	1.8V	0.2A
VccVFM	1.8V	0.159A
Vcc3_3	3.3V	0.409A
VccADAC	3.3V	0.068A
VccSPI	3.3V	0.02A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.097A
VccSUSHDA	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
V5REF	5V	1mA
V5REF_SUS	5V	1mA

LAN INTEL_82579		
VDD3P3	3.3V	90mA
VDD1P0	1V	332mA
CTRL1P0 internal LVR Output		

SUPER I/O IT8728		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO ALC662-VC		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

Fans
12V_200mA

SPI
VCC3_30mA

CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x 2

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Battery
3V

X16 PCIE Slot per	
3.3V	3A(S0)
12V	5.5A(S0)
3.3Vaux	0.375A

X1 PCIE Slot per	
3.3V	3A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A

PCI Slot per	
5V	5A(S0)
12V	0.5A(S0)
3.3Vaux	0.375A
3.3V	7.6A(S0)

USB X4 Header	
VDD	5VDual
5VDual	2.0A

USB X4 IO	
VDD	5VDual
5VDual	2.0A

PS/2	
5VDual	1.0A

